

FM8 Hanks Intel Discrete GFX

VER : 3A
PWA:W021J
PWB:W018J

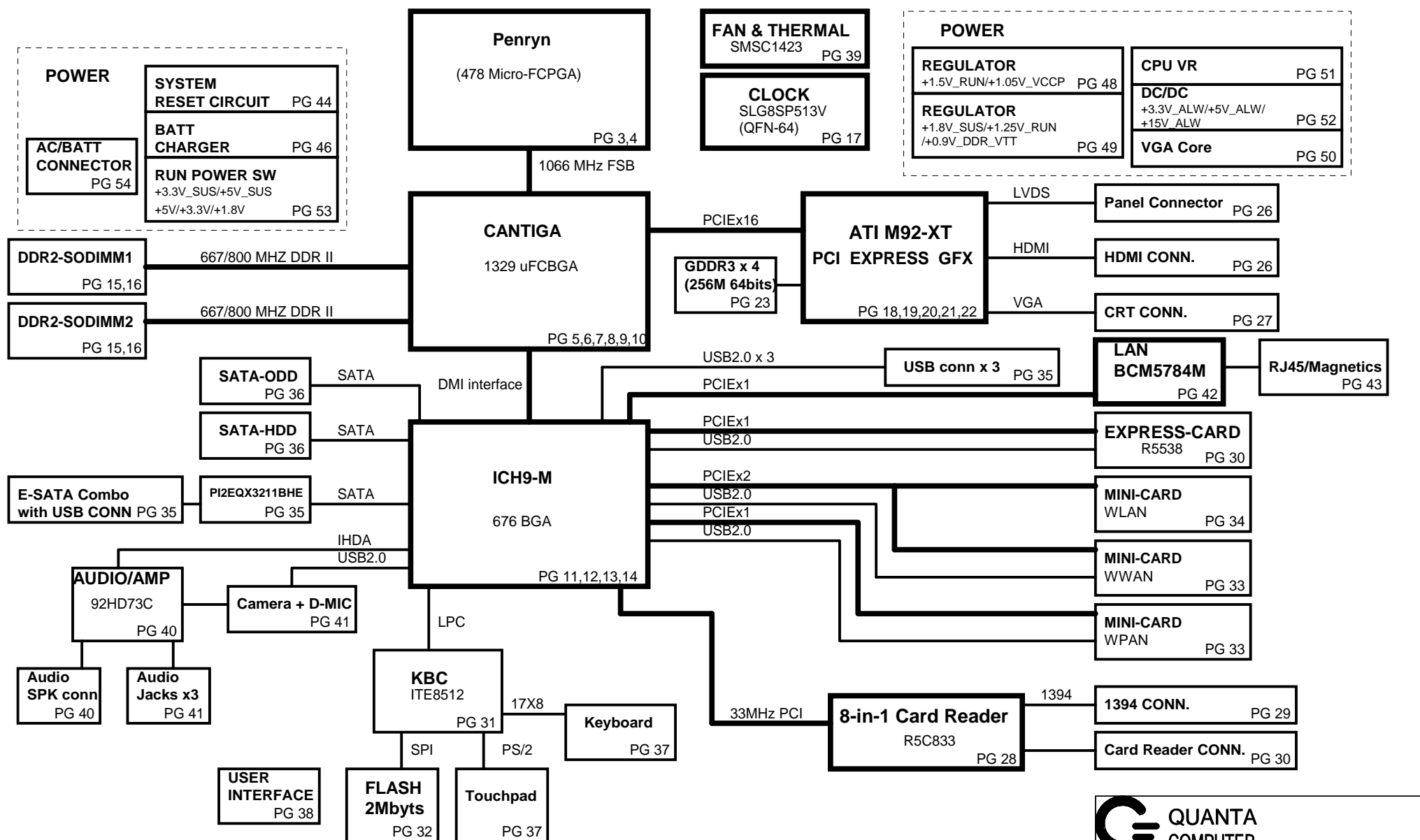









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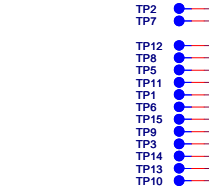
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Power States

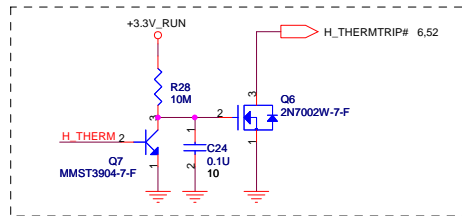
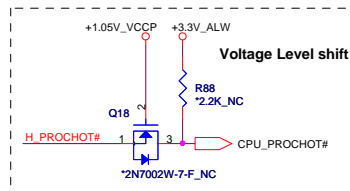
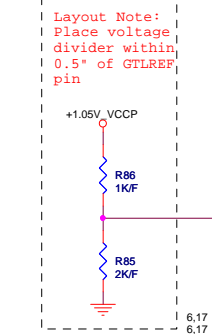
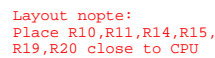
POWER PLANE	VOLTAGE	PAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
+PWR_SRC	10V~+19V	4,26,32,34,46,48,49,50,51,52	MAIN POWER		S0~S5
+RTC_CELL	+3.0V~+3.3V	11,14,31,32	RTC		S0~S5
+3.3V_ALW	+3.3V	3,13,31,32,36,37,38,44,46,49,52,53,54	8051 POWER	ALWON	S0~S5
+5V_ALW2	+5V	38,48,49,52,53,54	LARGE POWER	RUN_ON	S0~S5
+3.3V_LAN	+3.3V	42,43	LAN POWER	AUX_ON	
+5V_SUS	+5V	14,35,36,38,50,51,52,53	SLP_S5# CTRLD POWER	SUS_ON	
+3.3V_SUS	+3.3V	3,11,12,13,14,20,26,30,38,43,48,50,51,53	SLP_S5# CTRLD POWER	SUS_ON	
+1.8V_SUS	+1.8V	6,8,9,15,48,49,50,53	SODIMM POWER	SUS_ON	
+0.9V_DDR_VTT	+0.9V	16,49,53	SODIMM POWER	RUN_ON	
+5V_RUN	+5V	14,20,26,27,36,37,39,40,41,53	SLP_S3# CTRLD POWER	RUN_ON	
+3.3V_RUN	+3.3V	3,6,8,9,11,12,13,14,15,17,20,22,26,27,28,30,31,33,34,36,39,40,41,42,51,53	SLP_S3# CTRLD POWER	RUN_ON	
+1.8V_RUN	+1.8V	19,20,21,22,23,38,53	SDVO POWER	RUN_ON	
+1.5V_RUN	+1.5V	4,9,14,30,31,33,34,48,53	CALISTOGA/ICH9 POWER	RUN_ON	
+1.2V_LOM	+1.25V	42	LOM POWER	+3.3V_LAN	
+1.1V_GFX_PCIE	+1.1V	21,50	VGA POWER	RUN_ON	
+1.05V_VCCP	+1.05V	3,4,5,6,8,9,11,14,48	CPU/CALISTOGA/ICH8 POWER	1.05V_RUN_ON	
+VCC_CORE	+0.7V~+1.77V	4,51	CPU CORE POWER	IMVP_VR_ON	
+LCDVCC	+3.3V	26	LCD Power	LCDVCC_TST_EN & ENVDD	
+5V_MOD	+5V	36	Module Power	MODC_EN	
+5V_HDD	+5V	36	HDD Power	HDDC_EN	

GND PLANE	PAGE	DESCRIPTION
 GND_CHG	46	
 GND_1.05V	47	
 GND_VGA	50	
 GND_SIGNAL	51	
 AGND_DC/DC	52	
 GND	ALL	

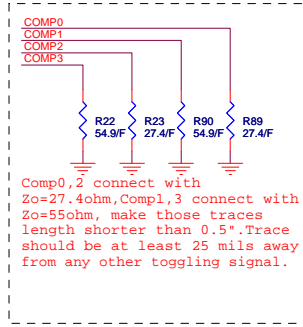
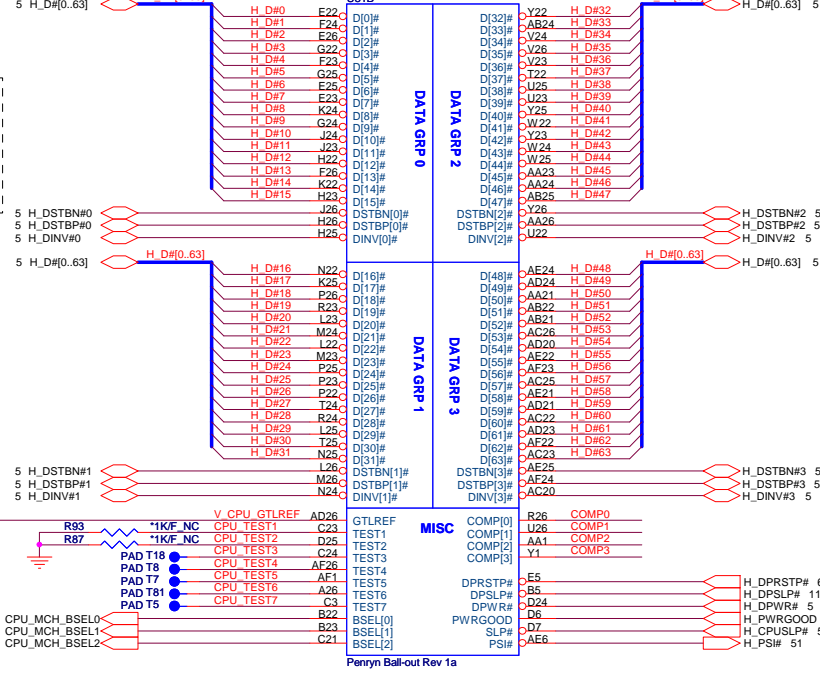
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Title: Index & Power Status		
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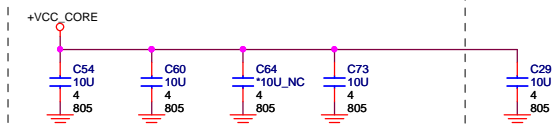
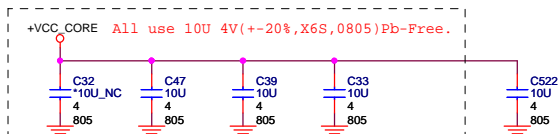
Populate ITP700Flex for bringup



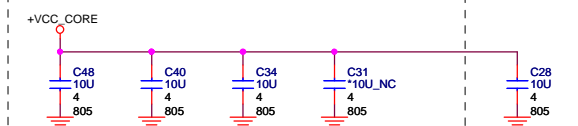
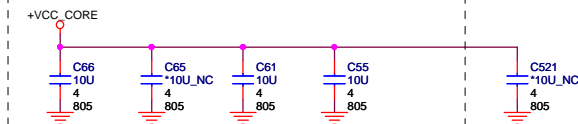
ITP disable guidelines			
Signal	Resistor Value	Connect To	Resistor Placement
TDI	150 ohm +/- 5%	VTT	Within 2.0" of the ITP
TMS	39 ohm +/- 5%	VTT	Within 2.0" of the ITP
TRST#	680 ohm +/- 5%	GND	Within 2.0" of the ITP
TCK	27 ohm +/- 5%	GND	Within 2.0" of the ITP
TDO	Open	VTT	Within 2.0" of the ITP
ITP_EN	R268 Depop	+3VRUN	Close to CK410M Pin8



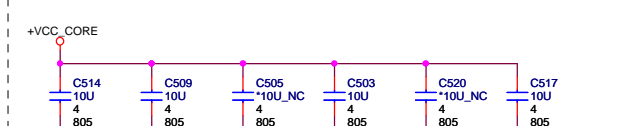
FSB	BCLK	BSEL2	BSEL1	BSEL0
533	133	0	0	1
667	166	0	1	1
800	200	0	1	0
1066	266	0	0	0



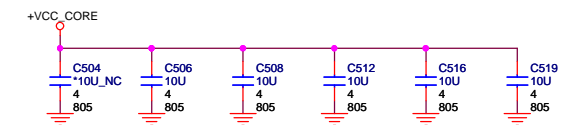
8 inside cavity, north side, secondary layer.



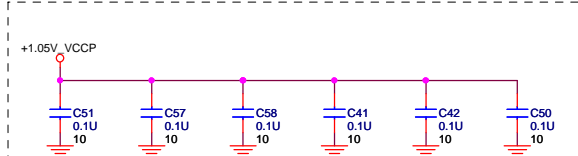
8 inside cavity, south side, secondary layer.



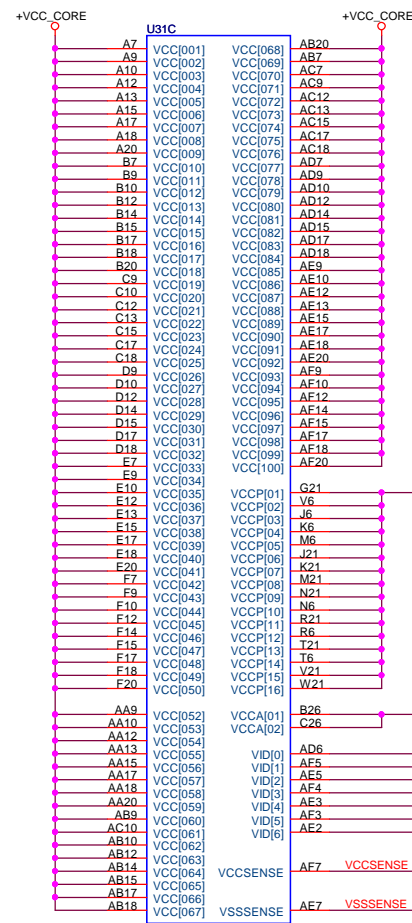
6 inside cavity, north side, primary layer.



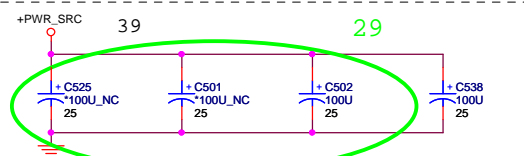
6 inside cavity, south side, primary layer.



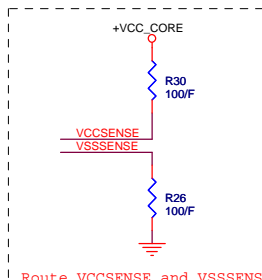
Layout out:
Place these inside socket cavity on North side secondary.



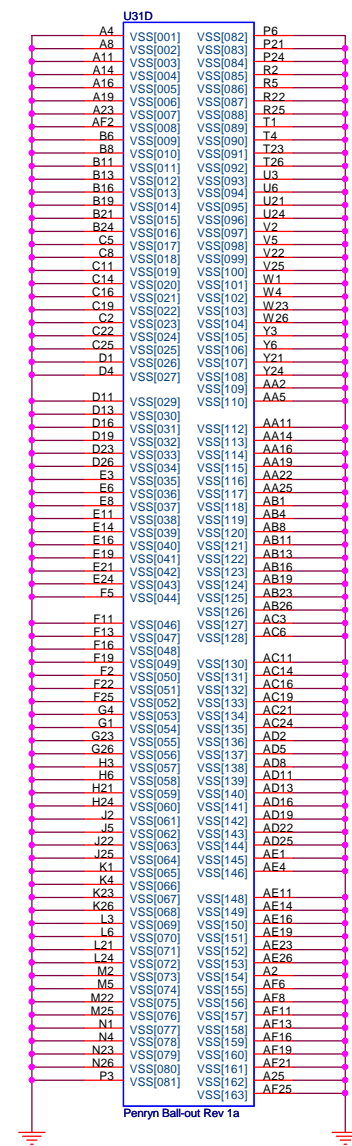
Penryn Ball-out Rev 1a



Layout Note:
Need to add 100uF cap on PWR_SRC for cap singing.
Place on PWR_SRC near +VCC_CORE.



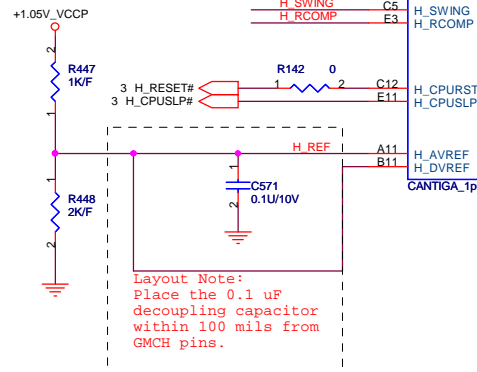
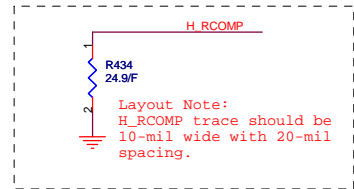
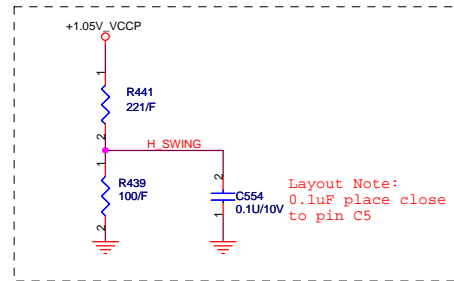
Route VCCSENSE and VSSSENSE traces at 27.4ohms and length matched to within 25 mil. Place PU and PD within 2 inch of CPU.



Penryn Ball-out Rev 1a

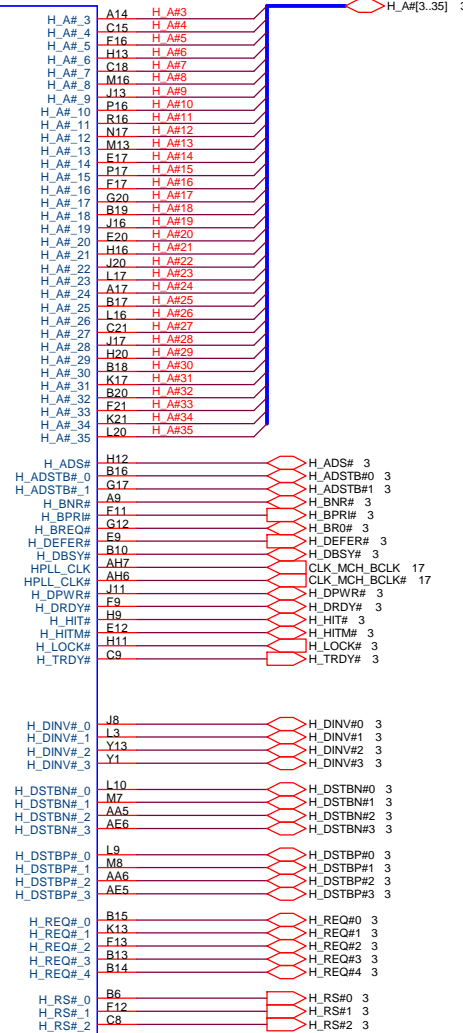


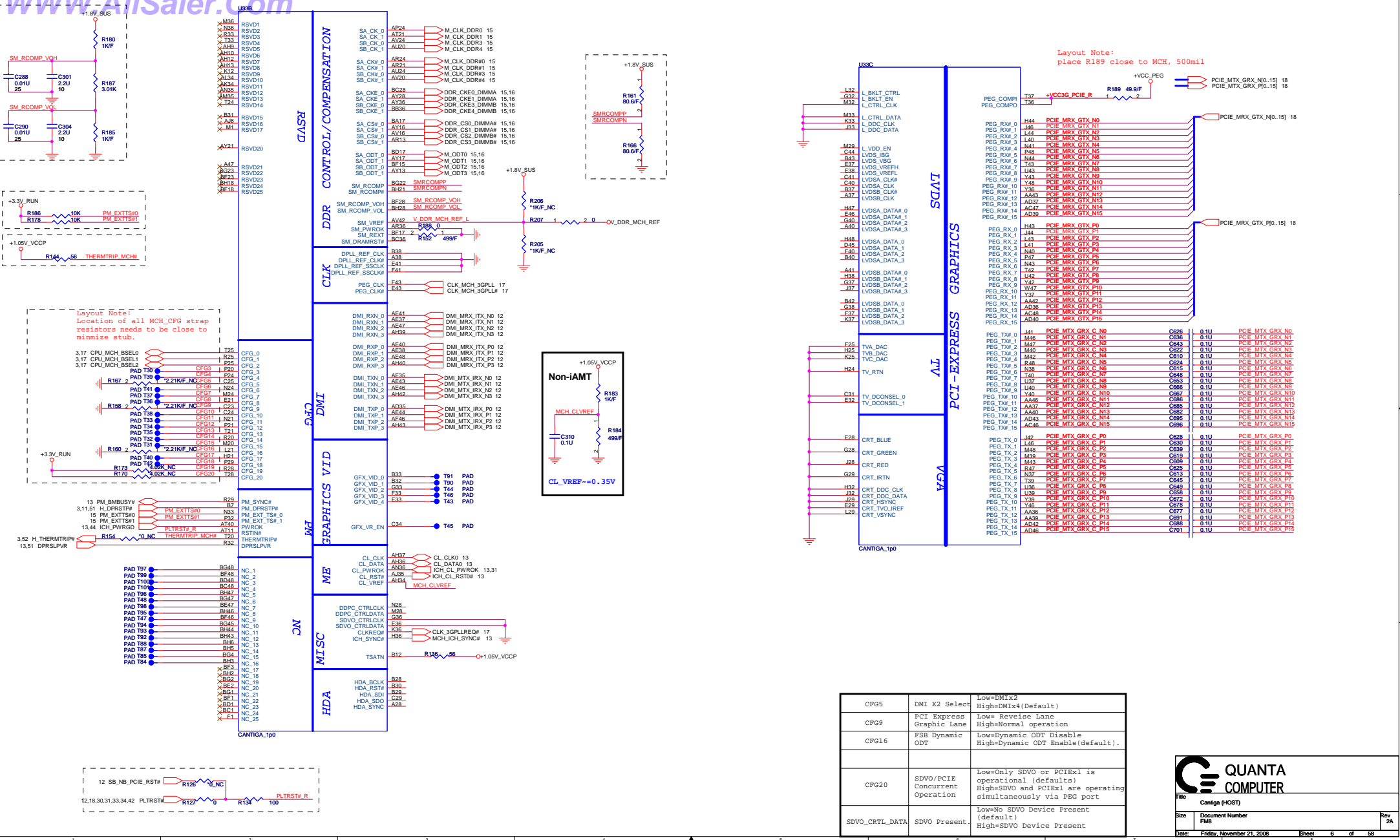
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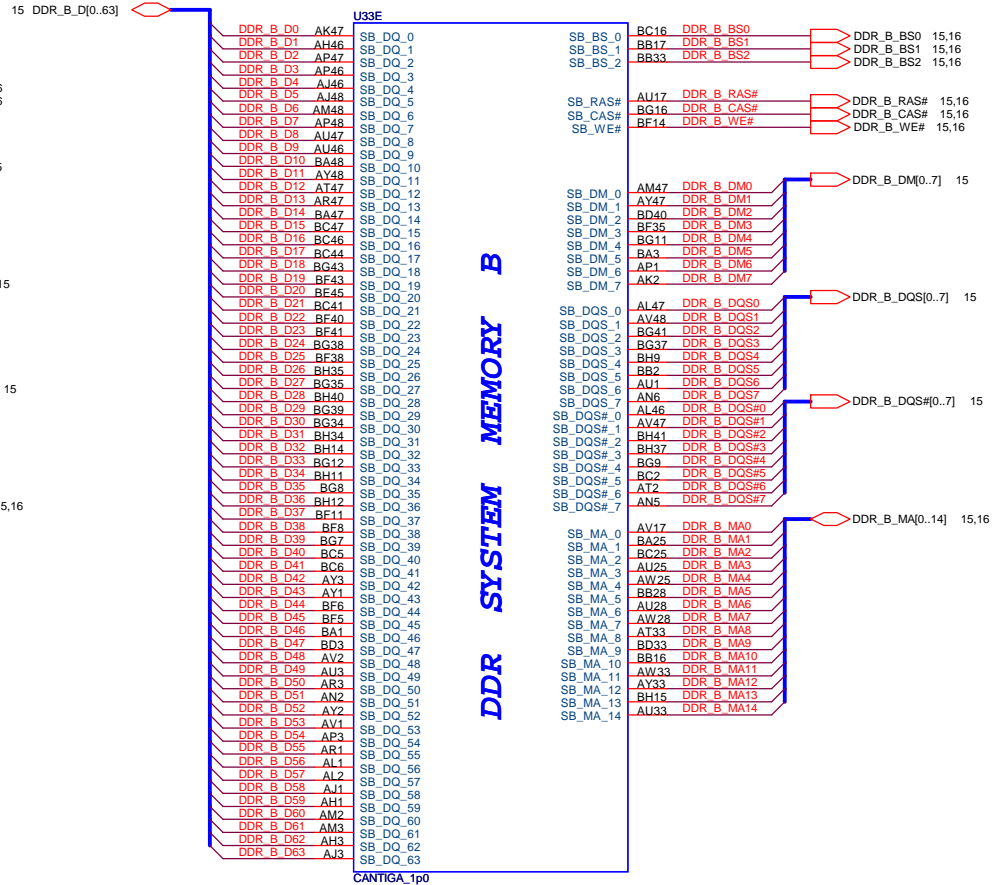
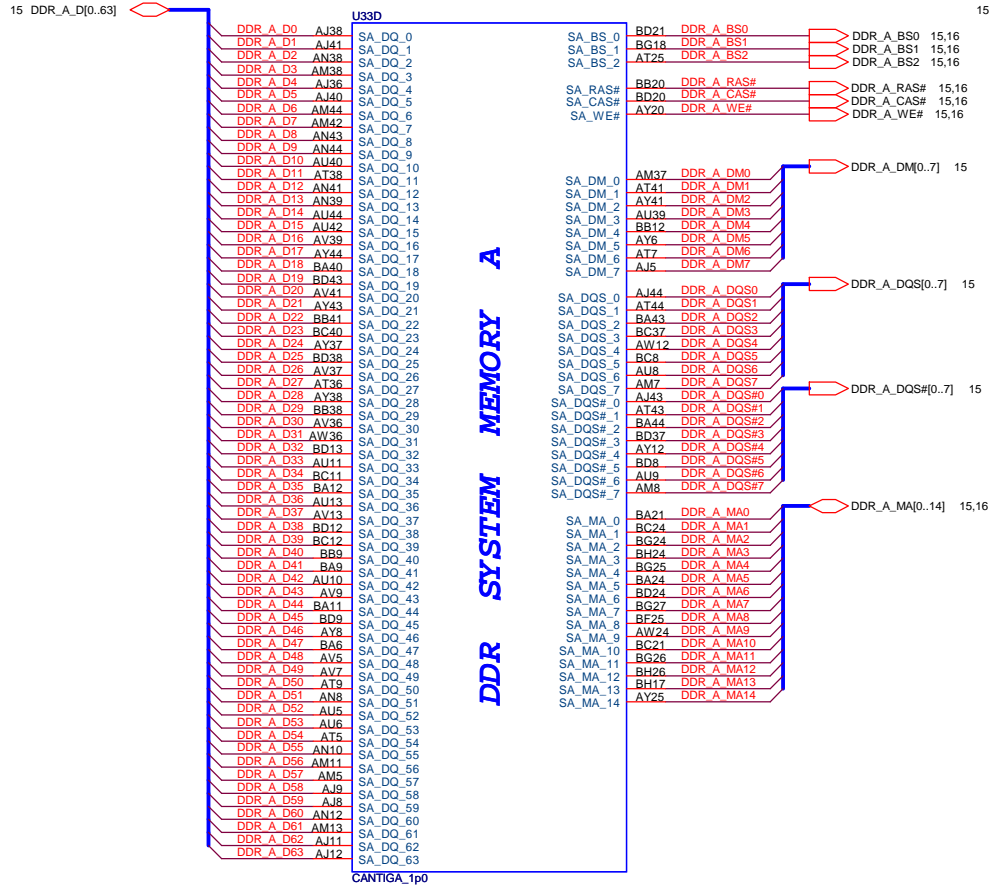



U33A

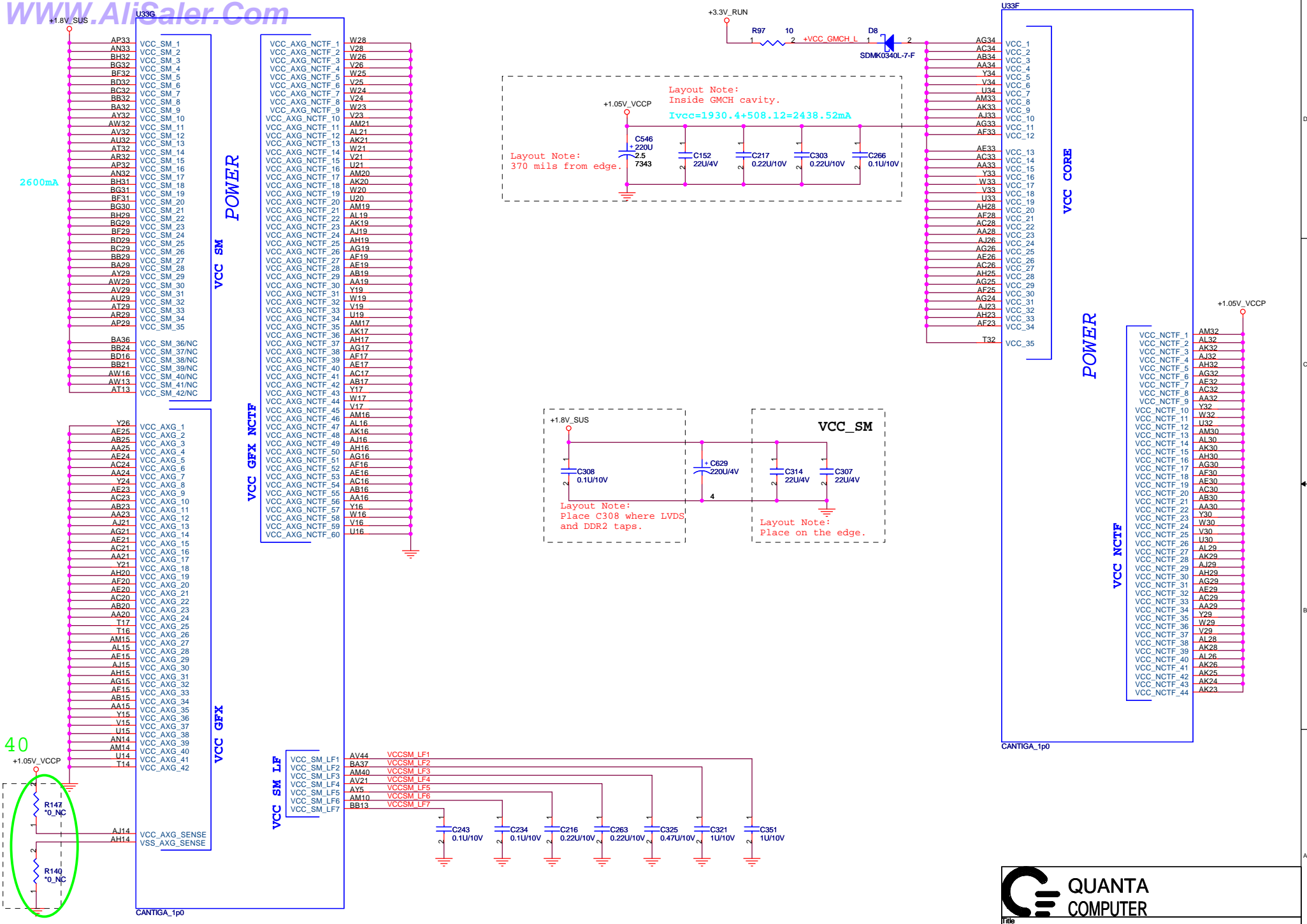
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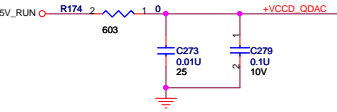
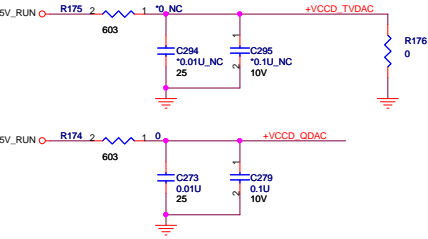
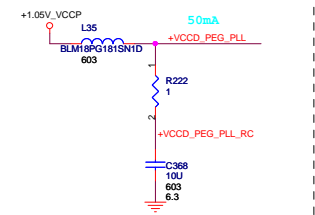
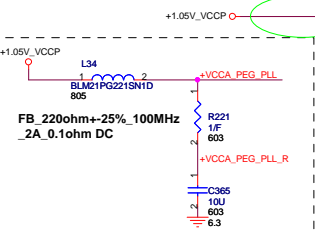
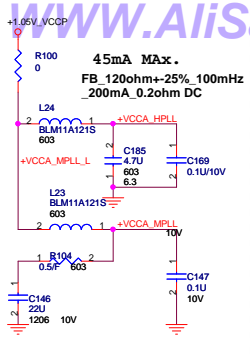






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Title Cantiga (HOST)		
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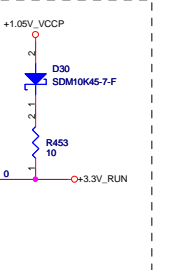
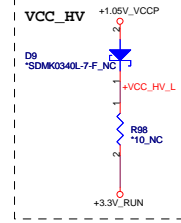
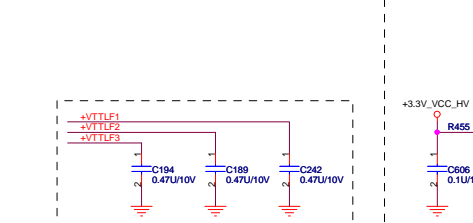
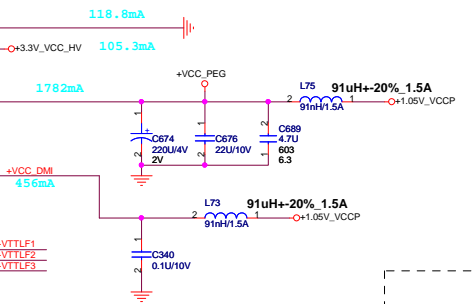
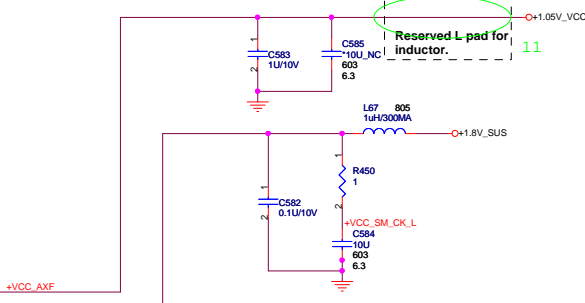
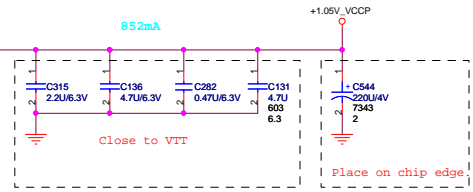
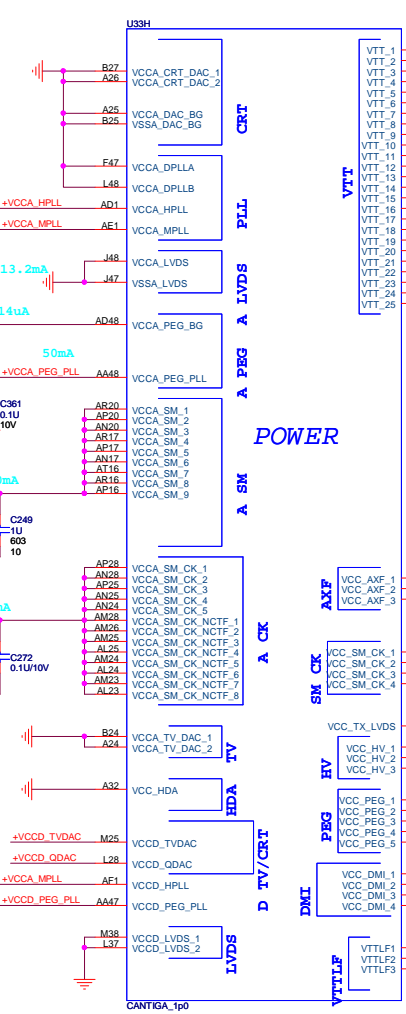
AB total 64.8mA
24mA
139.2mA

1.5V_RUN
414uA
50mA

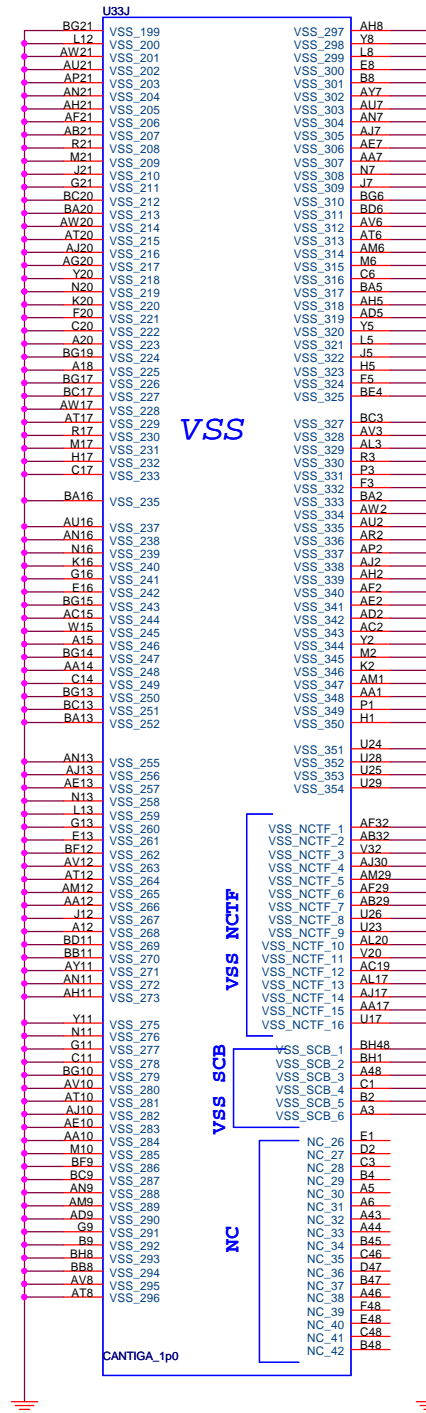
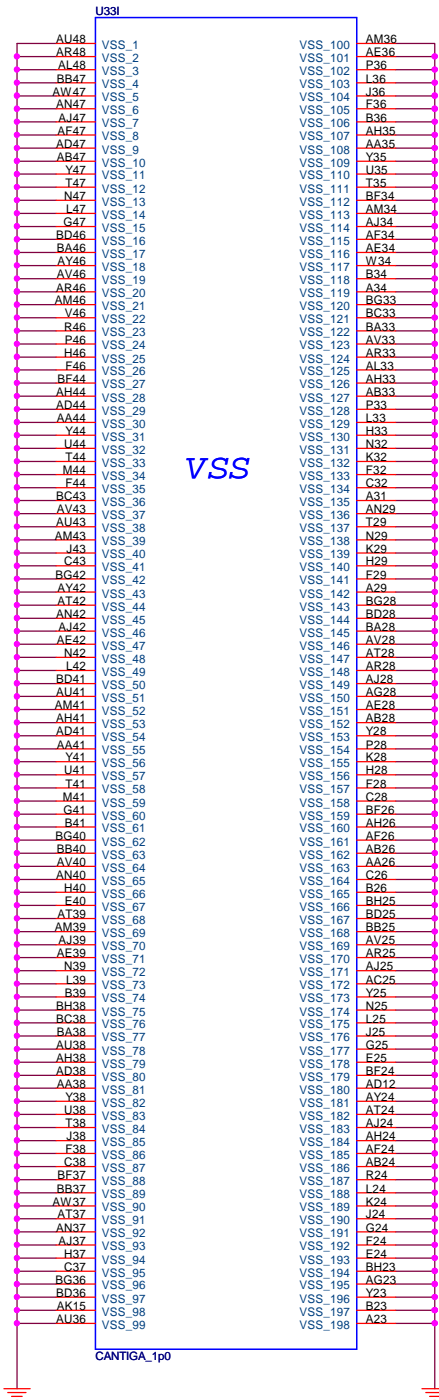
480mA

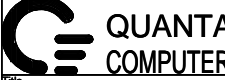
1uH+-20%_300mA
24mA

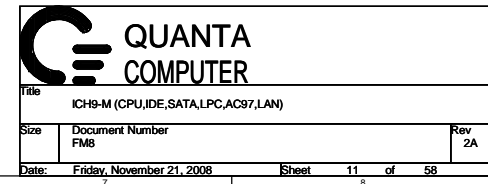
157.2mA



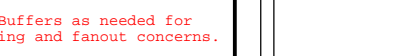
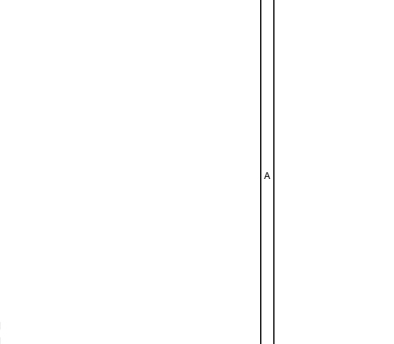
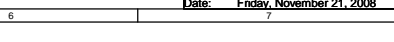
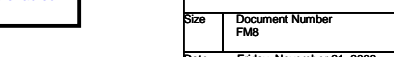
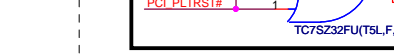
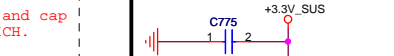
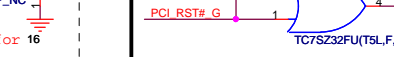
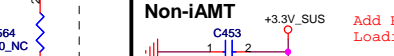
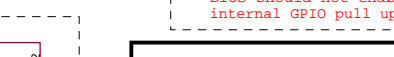
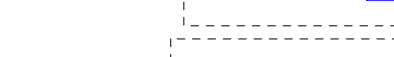
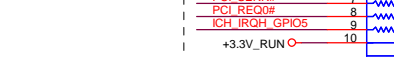
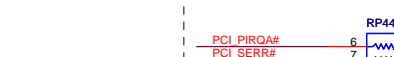
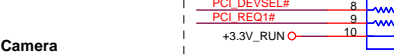
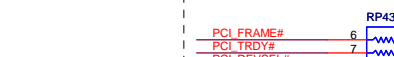
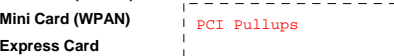
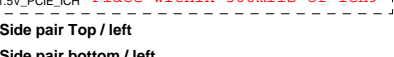
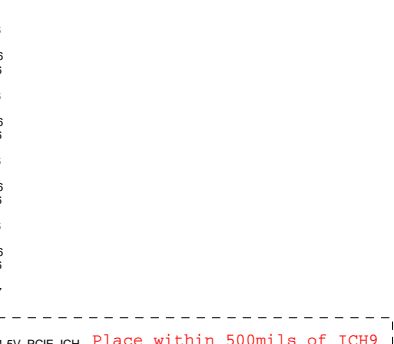
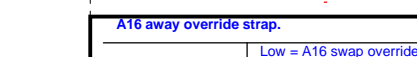
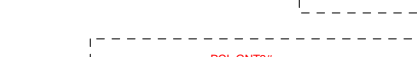
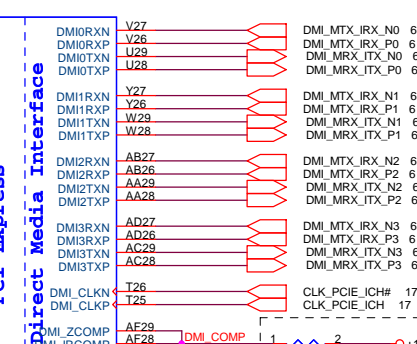
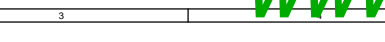
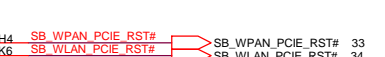
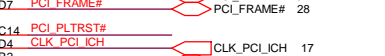
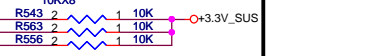
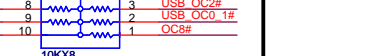
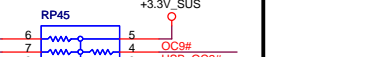
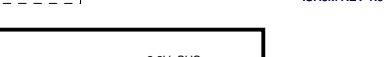
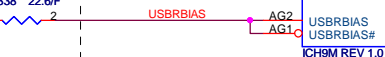
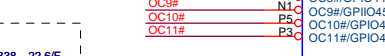
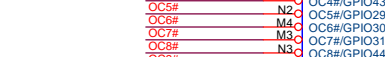
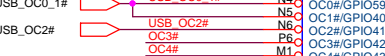
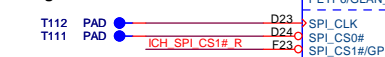
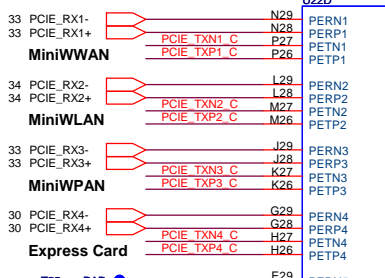
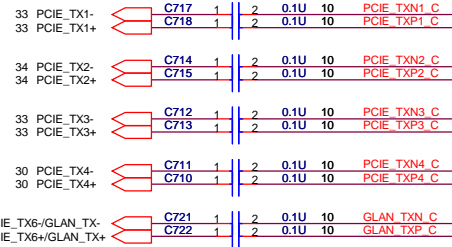
File	Cantiga (HOST)	Rev	2A
Size	Document Number		
	FMB		
Date	Friday, November 21, 2008	Sheet	9 of 58

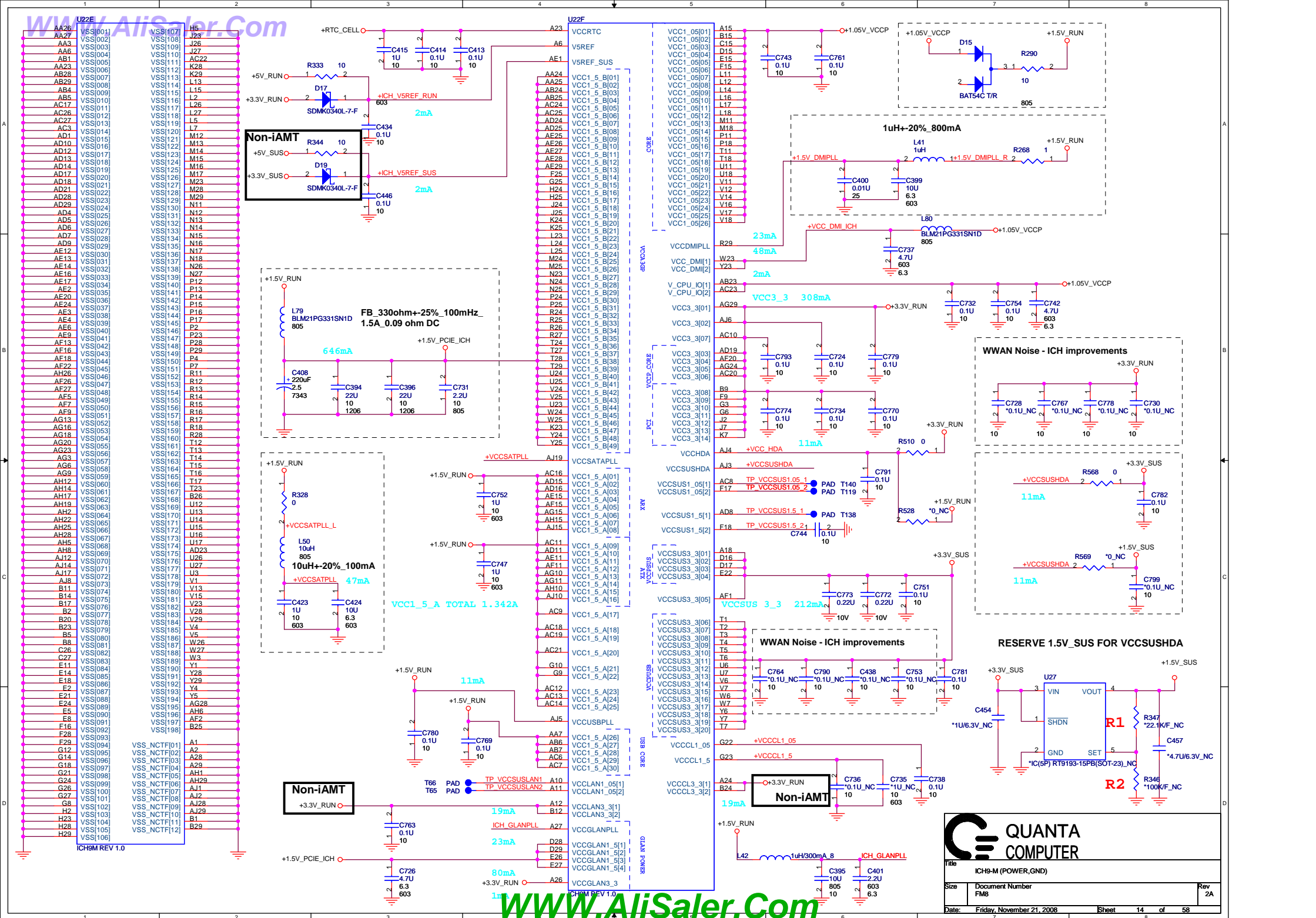


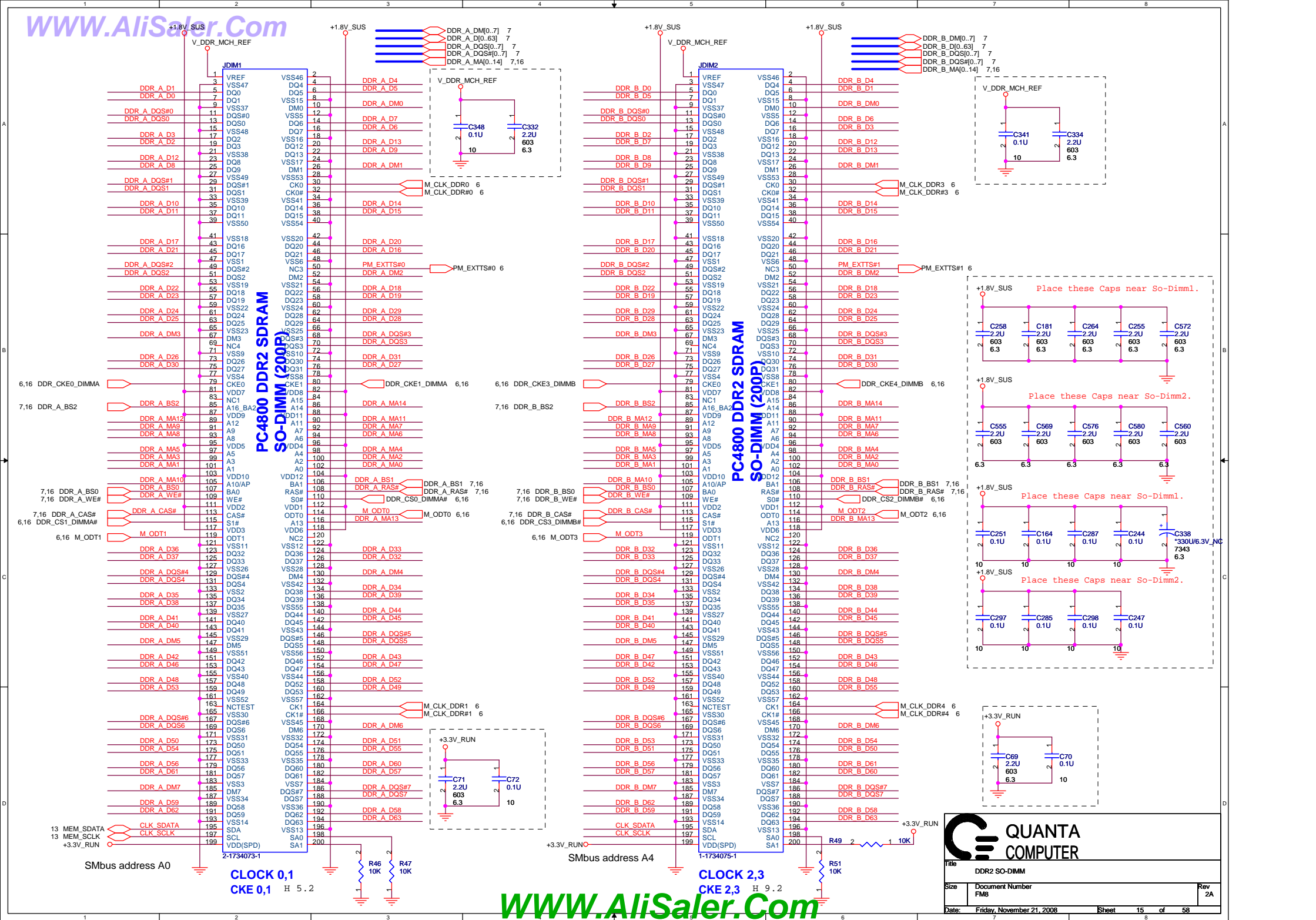
		
Title Cantiga (HOST)		
Size	Document Number FM8	Rev 2A
Date: Friday, November 21, 2008	Sheet 10	of 58

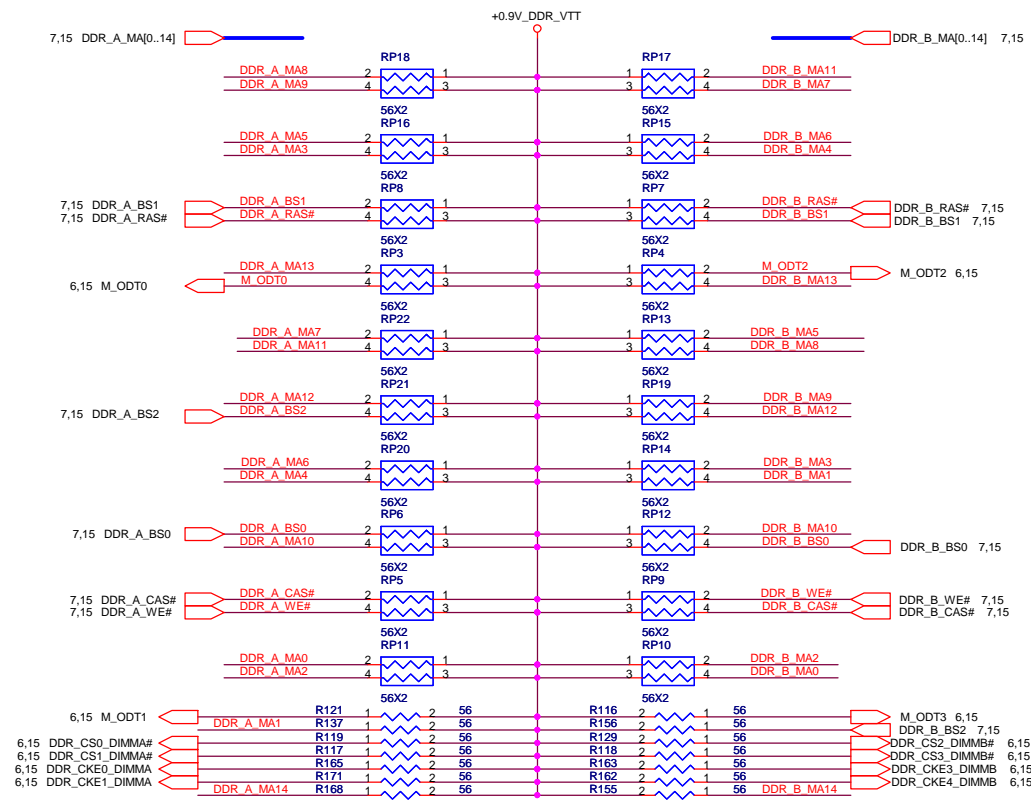
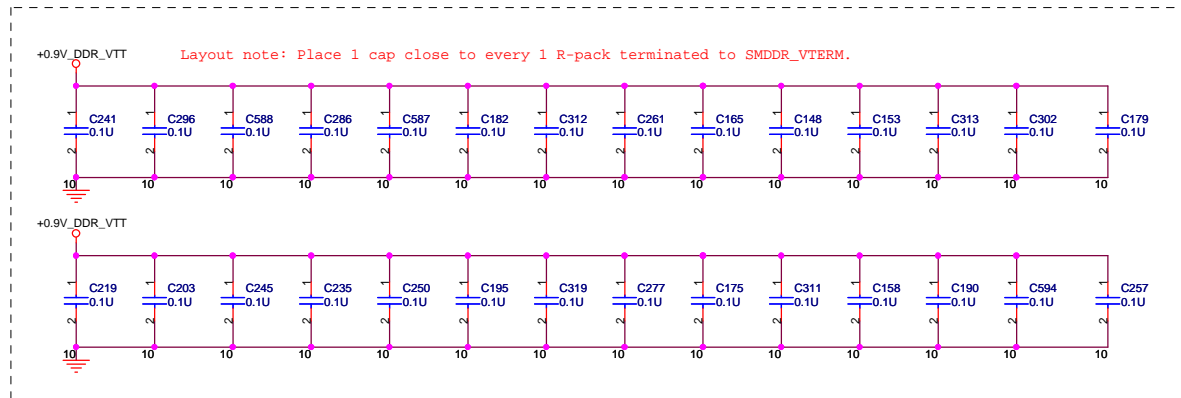


Place TX DC blocking caps close ICH9.







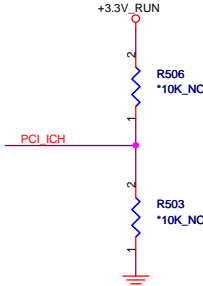
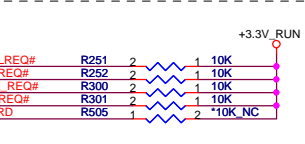
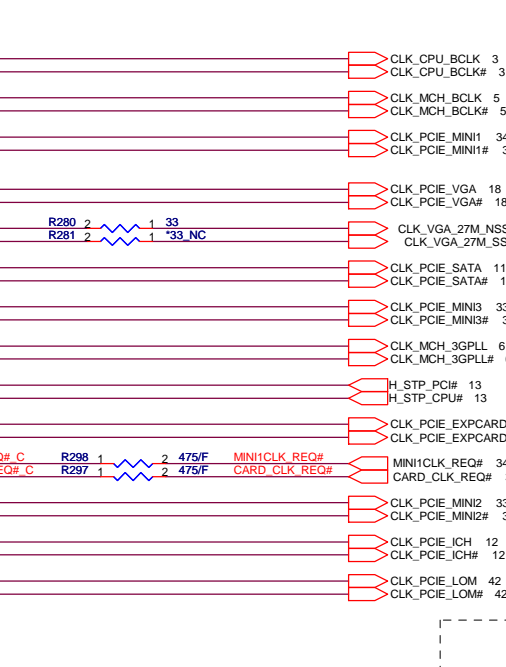
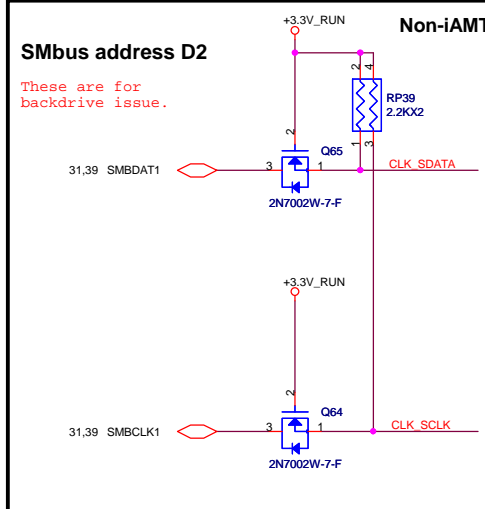
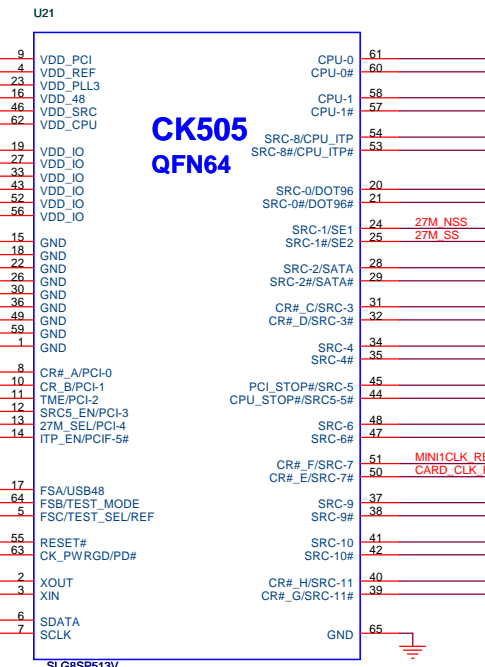
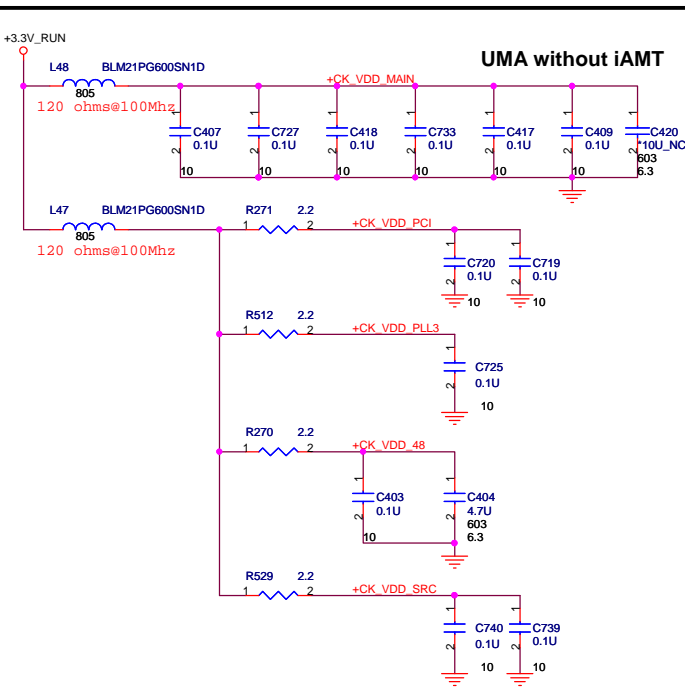
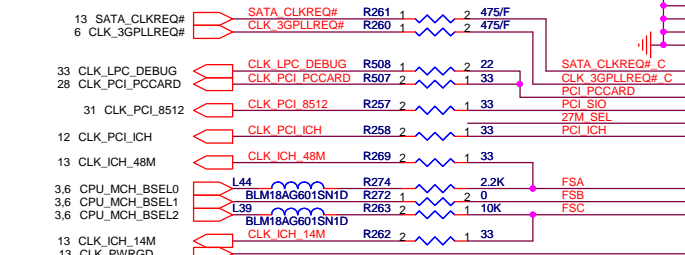
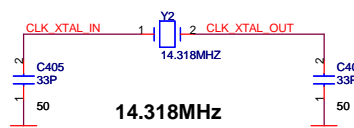
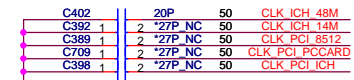


Layout notice:
Please these resistor
closely DIMMA,all
trace length<750 mil.

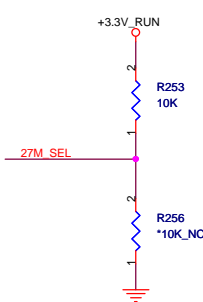
Layout notice:
Please these resistor
closely DIMMB,all
trace length<750 mil.

Title: DDR2 RES. ARRAY		
Size: FMS	Document Number: 2A	Rev: 2A
Date: Friday, November 21, 2008	Sheet: 16	of 58

Add capacitor pads for improving WWAN.



R506 POP: For Internal pull-low.
R503 POP: For internal pull-high.



FSC	FSB	FSA	CPU	SRC	PCI
1	0	1	100	100	33
0	0	1	133	100	33
0	1	1	166	100	33
0	1	0	200	100	33
0	0	0	266	100	33
1	0	0	333	100	33
1	1	0	400	100	33
1	1	1	RSVD	100	33

27M_SEL

27M_SEL (PIN13)	PIN20	PIN21	PIN24	PIN25
0=UMA	DOT96T	DOT96C	96/100M_T	96/100M_C
1 = Disc. GRFX down	SRCT0	SRCC0	27Mout	27MSSout



File: CLOCK GENERATOR

Size: Document Number: FMS Rev: 2A

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6 PCIE_MTX_GRX_P[0..15]
6 PCIE_MTX_GRX_N[0..15]

PCIE_MTX_GRX_P0 AF30
PCIE_MTX_GRX_N0 AE31

PCIE_MTX_GRX_P1 AE29
PCIE_MTX_GRX_N1 AD28

PCIE_MTX_GRX_P2 AD30
PCIE_MTX_GRX_N2 AC31

PCIE_MTX_GRX_P3 AC29
PCIE_MTX_GRX_N3 AB28

PCIE_MTX_GRX_P4 AB30
PCIE_MTX_GRX_N4 AA31

PCIE_MTX_GRX_P5 AA29
PCIE_MTX_GRX_N5 Y28

PCIE_MTX_GRX_P6 Y30
PCIE_MTX_GRX_N6 W31

PCIE_MTX_GRX_P7 W28
PCIE_MTX_GRX_N7 V28

PCIE_MTX_GRX_P8 V30
PCIE_MTX_GRX_N8 U31

PCIE_MTX_GRX_P9 U29
PCIE_MTX_GRX_N9 T28

PCIE_MTX_GRX_P10 T30
PCIE_MTX_GRX_N10 R31

PCIE_MTX_GRX_P11 R29
PCIE_MTX_GRX_N11 P28

PCIE_MTX_GRX_P12 P30
PCIE_MTX_GRX_N12 N31

PCIE_MTX_GRX_P13 N29
PCIE_MTX_GRX_N13 M28

PCIE_MTX_GRX_P14 M30
PCIE_MTX_GRX_N14 L31

PCIE_MTX_GRX_P15 L29
PCIE_MTX_GRX_N15 K30

100 MHz (+/-300 ppm) input frequency, 0-0.7 V single-ended swing.
clock must be provided less than 400ns
after CLKREQ# is asserted

17 CLK_PCIE_VGA
17 CLK_PCIE_VGA#

13 PLTRST_DELAY#

6,12,30,31,33,34,42 PLTRST#

43

U32A

PART 1 OF 10

PCI-EXPRESS INTERFACE

PCIE_REFCLKP AK30
PCIE_REFCLKN AK32

PERSTB AL27
M92-S2M92-XT

PCIE_TX0P AH30
PCIE_TX0N AG31

PCIE_TX1P AG29
PCIE_TX1N AF28

PCIE_TX2P AF27
PCIE_TX2N AF26

PCIE_TX3P AD27
PCIE_TX3N AD26

PCIE_TX4P AC25
PCIE_TX4N AB25

PCIE_TX5P Y23
PCIE_TX5N Y24

PCIE_TX6P AB27
PCIE_TX6N AB26

PCIE_TX7P Y27
PCIE_TX7N Y26

PCIE_TX8P W24
PCIE_TX8N W23

PCIE_TX9P V27
PCIE_TX9N U26

PCIE_TX10P U24
PCIE_TX10N U23

PCIE_TX11P T26
PCIE_TX11N T27

PCIE_TX12P T24
PCIE_TX12N T23

PCIE_TX13P P27
PCIE_TX13N P26

PCIE_TX14P P24
PCIE_TX14N P23

PCIE_TX15P M27
PCIE_TX15N M26

M92-S2 XT AJ072800T04 100-CG1675(216-0728004)
M92-S2 AJ072800T03 100-CG1643(216-0728003)

6 PCIE_MRX_GTX_P[0..15]
6 PCIE_MRX_GTX_N[0..15]

PCIE_MRX_GTX_P0 0.1U 2 1 C814 10 PCIE_MRX_GTX_C_P0
PCIE_MRX_GTX_P1 0.1U 2 1 C815 10 PCIE_MRX_GTX_C_P1
PCIE_MRX_GTX_P2 0.1U 2 1 C816 10 PCIE_MRX_GTX_C_P2
PCIE_MRX_GTX_P3 0.1U 2 1 C817 10 PCIE_MRX_GTX_C_P3
PCIE_MRX_GTX_P4 0.1U 2 1 C818 10 PCIE_MRX_GTX_C_P4
PCIE_MRX_GTX_P5 0.1U 2 1 C819 10 PCIE_MRX_GTX_C_P5
PCIE_MRX_GTX_P6 0.1U 2 1 C820 10 PCIE_MRX_GTX_C_P6
PCIE_MRX_GTX_P7 0.1U 2 1 C821 10 PCIE_MRX_GTX_C_P7
PCIE_MRX_GTX_P8 0.1U 2 1 C822 10 PCIE_MRX_GTX_C_P8
PCIE_MRX_GTX_P9 0.1U 2 1 C823 10 PCIE_MRX_GTX_C_P9
PCIE_MRX_GTX_P10 0.1U 2 1 C824 10 PCIE_MRX_GTX_C_P10
PCIE_MRX_GTX_P11 0.1U 2 1 C825 10 PCIE_MRX_GTX_C_P11
PCIE_MRX_GTX_P12 0.1U 2 1 C826 10 PCIE_MRX_GTX_C_P12
PCIE_MRX_GTX_P13 0.1U 2 1 C827 10 PCIE_MRX_GTX_C_P13
PCIE_MRX_GTX_P14 0.1U 2 1 C828 10 PCIE_MRX_GTX_C_P14
PCIE_MRX_GTX_P15 0.1U 2 1 C829 10 PCIE_MRX_GTX_C_P15

PCIE_MRX_GTX_N0 0.1U 2 1 C830 10 PCIE_MRX_GTX_C_N0
PCIE_MRX_GTX_N1 0.1U 2 1 C831 10 PCIE_MRX_GTX_C_N1
PCIE_MRX_GTX_N2 0.1U 2 1 C832 10 PCIE_MRX_GTX_C_N2
PCIE_MRX_GTX_N3 0.1U 2 1 C833 10 PCIE_MRX_GTX_C_N3
PCIE_MRX_GTX_N4 0.1U 2 1 C834 10 PCIE_MRX_GTX_C_N4
PCIE_MRX_GTX_N5 0.1U 2 1 C835 10 PCIE_MRX_GTX_C_N5
PCIE_MRX_GTX_N6 0.1U 2 1 C836 10 PCIE_MRX_GTX_C_N6
PCIE_MRX_GTX_N7 0.1U 2 1 C837 10 PCIE_MRX_GTX_C_N7
PCIE_MRX_GTX_N8 0.1U 2 1 C838 10 PCIE_MRX_GTX_C_N8
PCIE_MRX_GTX_N9 0.1U 2 1 C839 10 PCIE_MRX_GTX_C_N9
PCIE_MRX_GTX_N10 0.1U 2 1 C840 10 PCIE_MRX_GTX_C_N10
PCIE_MRX_GTX_N11 0.1U 2 1 C841 10 PCIE_MRX_GTX_C_N11
PCIE_MRX_GTX_N12 0.1U 2 1 C842 10 PCIE_MRX_GTX_C_N12
PCIE_MRX_GTX_N13 0.1U 2 1 C843 10 PCIE_MRX_GTX_C_N13
PCIE_MRX_GTX_N14 0.1U 2 1 C844 10 PCIE_MRX_GTX_C_N14
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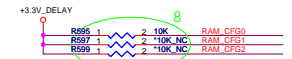
(1.1V)
+PCIE_VDDC

PCIE_CALRN AA22 PCIE_CALRN 2.0K R591
PCIE_CALRP Y22 PCIE_CALRP 1.27K R592

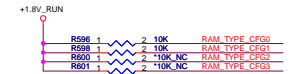
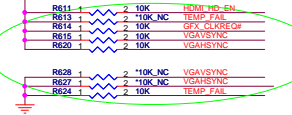
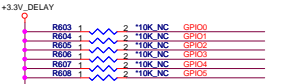


Title		
VGA-M92-XT (PCIe)		
Size	Document Number	Rev
FM8		2A
Date:	Friday, November 21, 2008	Sheet 18 of 58

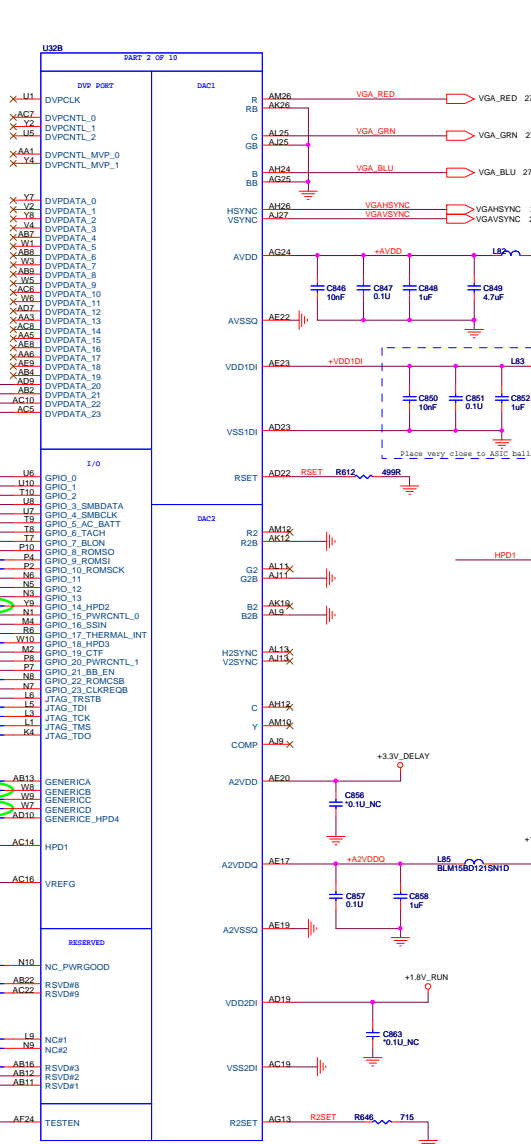
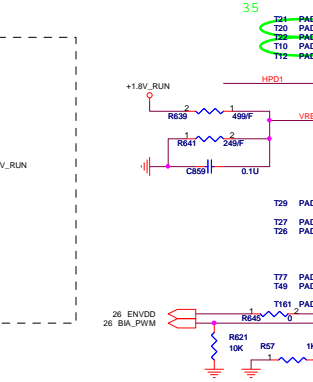
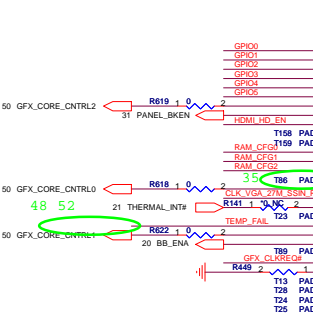
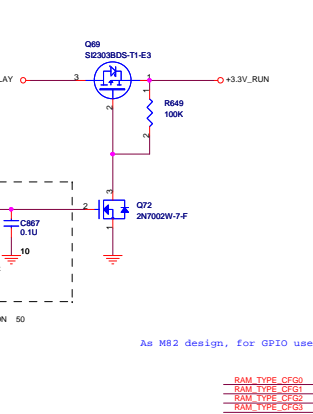
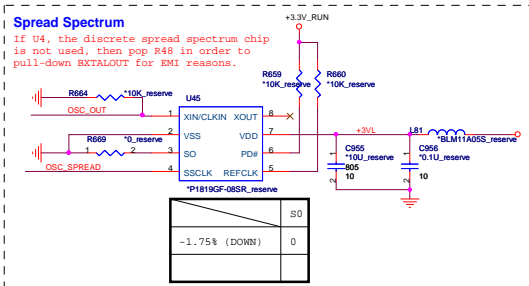
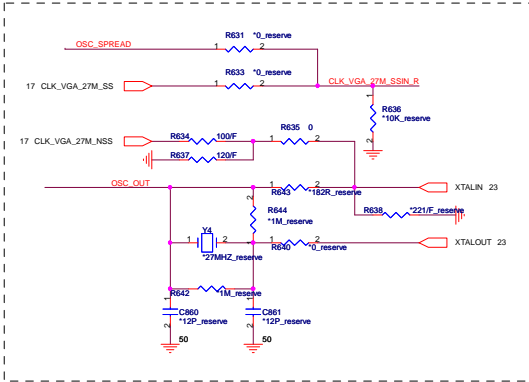
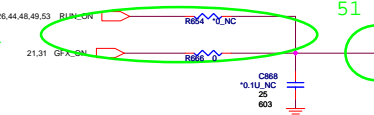
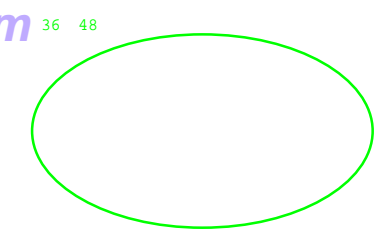
MEMORY APERTURE SIZE SELECT				
MEMORY SIZE	CFG3 GP109	CFG2 GP1013	CFG1 GP1012	CFG0 GP1011
128MB	0	0	0	0
256MB	0	0	0	1
64MB	0	0	1	0
512MB	1	0	0	0

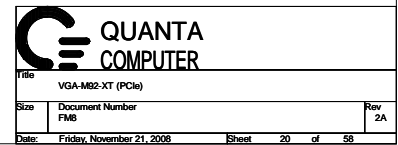


GPIO Straps Table	DESCRIPTION OF DEFAULT SETTINGS	FM8 setting
GPIO0	GPIO0 - TX_PRRS_EN (Transmitter Power Savings Enable) 0: 50% Tx output swing for mobile mode 1: full Tx output swing (Default setting for Desktop)	0
GPIO1	GPIO1 - TX_DEEMPH_EN (Transmitter De-emphasis Enable) 0: Tx de-emphasis disabled for mobile mode 1: Tx de-emphasis enabled (Default setting for Desktop)	0
GPIO2	GPIO2 - BIF_GEN2_EN (5.0 GT/s Enable) 0: Default (Driver Controlled Gen2) 1: Strap Controlled Gen2	0
GPIO3	ATI reserved configuration straps.	0
GPIO4	ATI reserved configuration straps.	0
GPIO5	GPIO_5_AC_BATT 0: Battery saving mode = 0.9 V 1: AC (Performance mode) = 3.3 V	0
GPIO6	ATI Internal use only	0

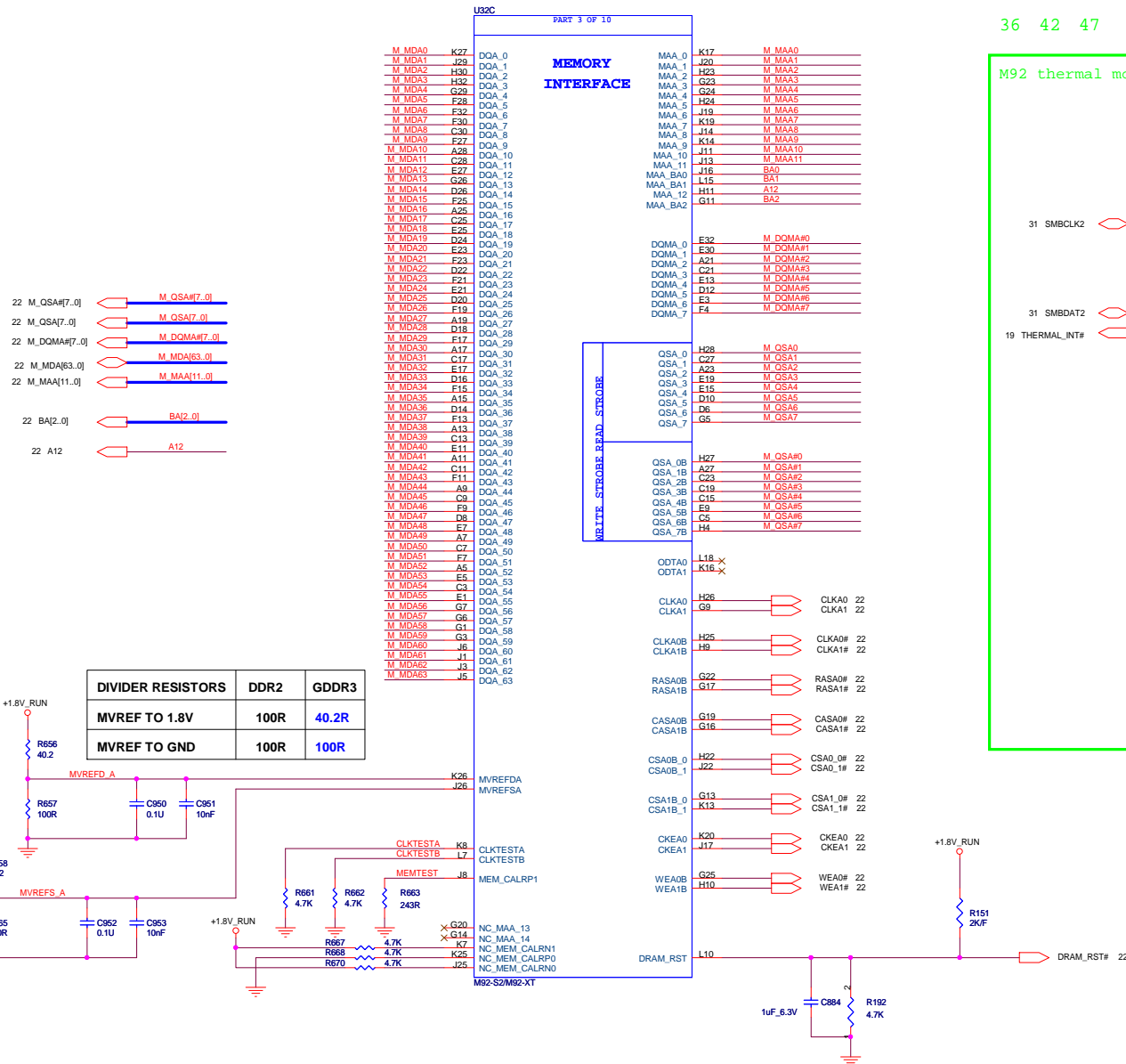


Memory Straps	RAM_TYPE_CFG3	RAM_TYPE_CFG2	RAM_TYPE_CFG1	RAM_TYPE_CFG0	Quanta PN (QuantaBuy)	Quanta PN (WinBuy)	Vendor PN	31 level PN
800MHz 512MB(32M*32) Samsung	0	0	1	0	AKD5LWGT501	AKD5LWGT504	K4J10324QD-HC12	31FM8MB0030
900MHz 512MB(32M*32) Qimonda	0	0	1	1	AKD5LWFT*03	AKD5LWFT*00	HYB18H1G321AF-11	31FM8MB0000
800MHz 256MB(16M*32) Samsung	0	0	0	1	AKD5FWGT500	AKD5FWGT503	K4J52324QH-HC12	31FM8MB0040
900MHz 256MB(16M*32) Hynix	0	0	0	0	AKD5FWHTW03	AKD5FWHTW06	H5RS5223CFR-11C	31FM8MB0020



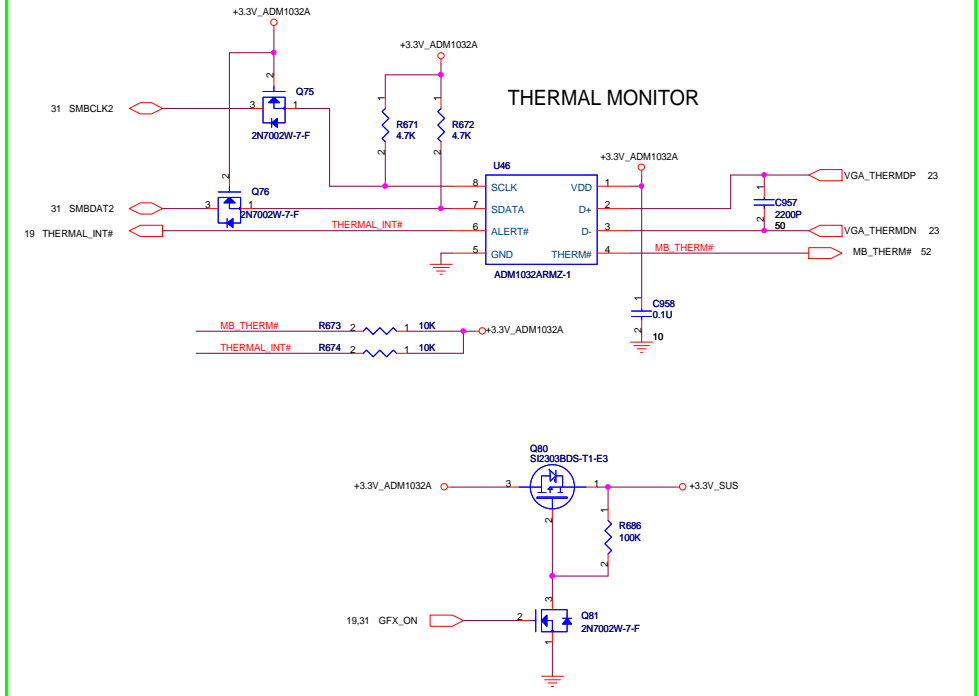


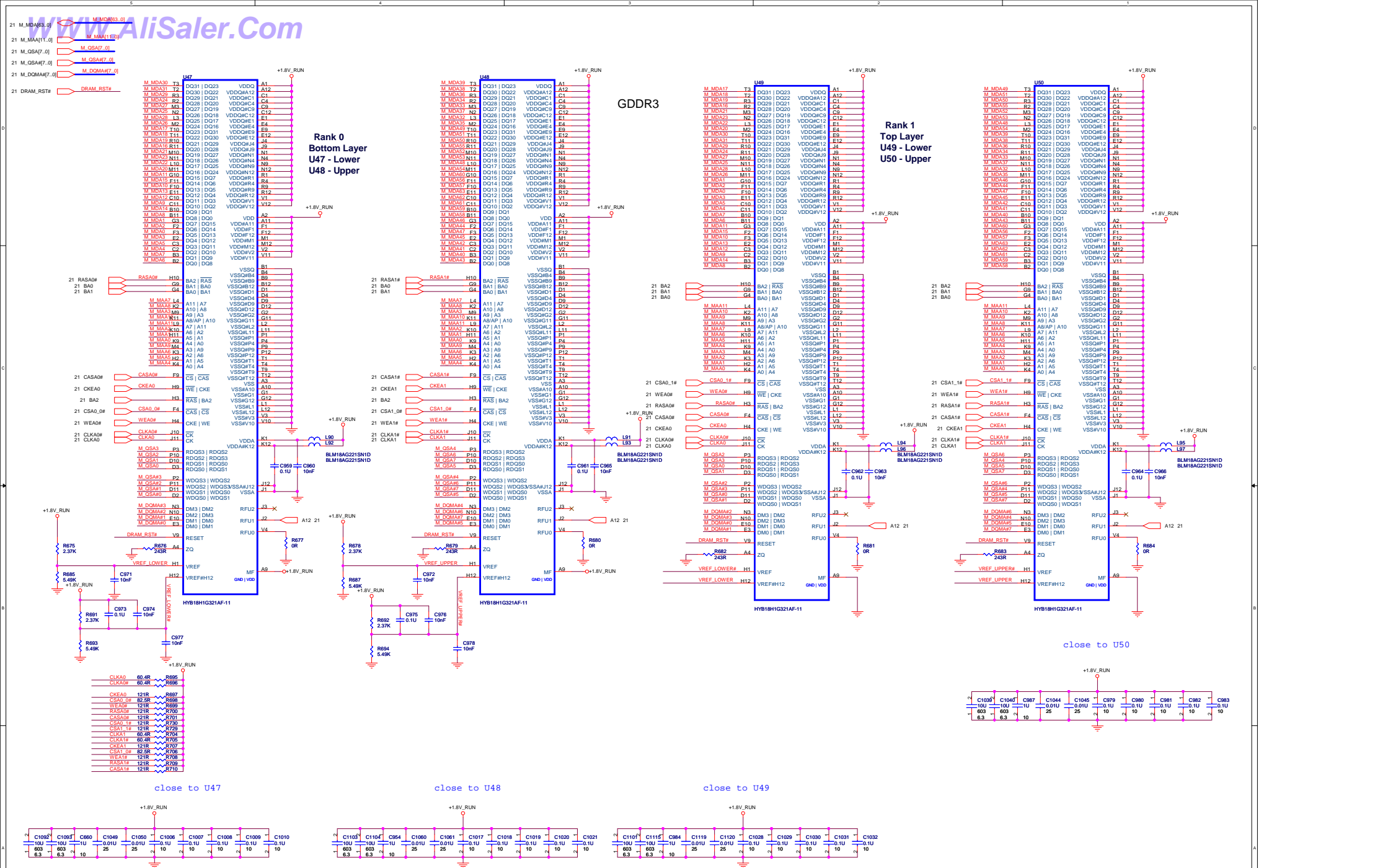
MEMORY INTERFACE

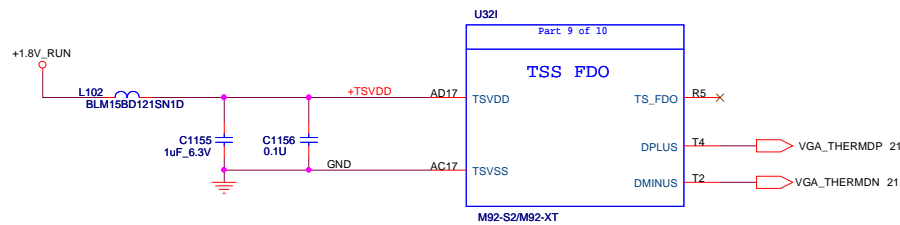
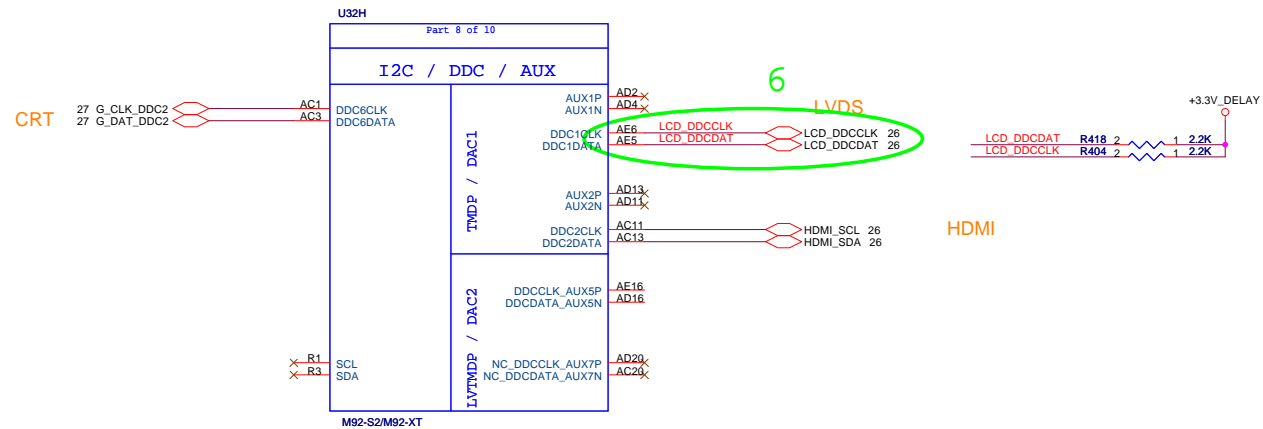
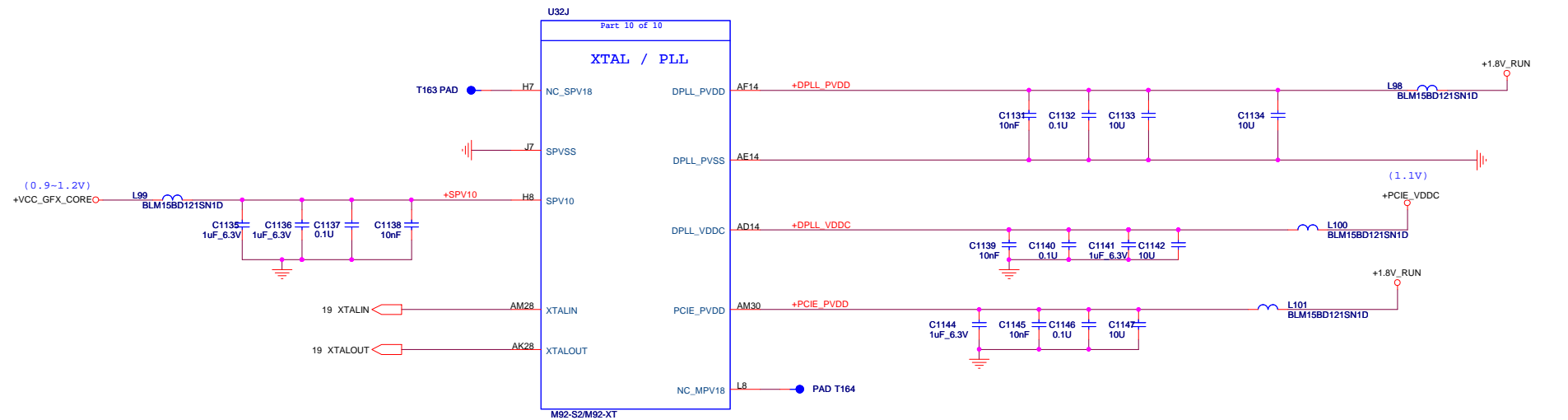


36 42 47

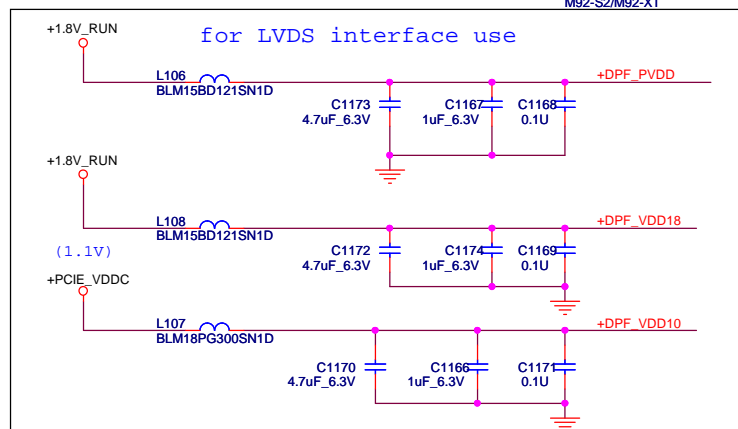
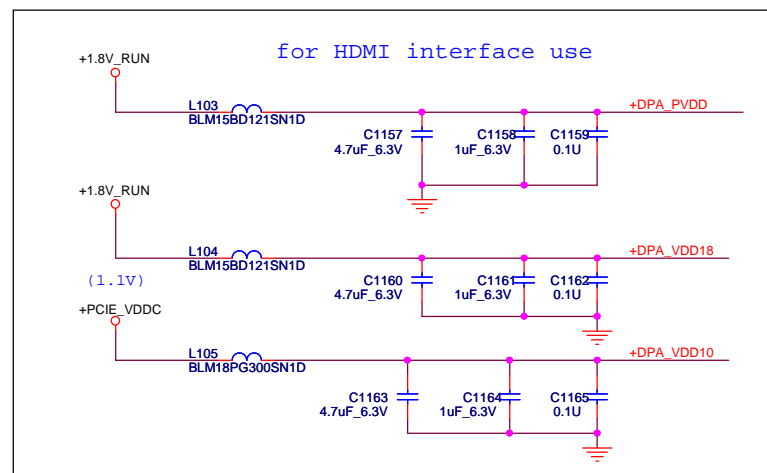
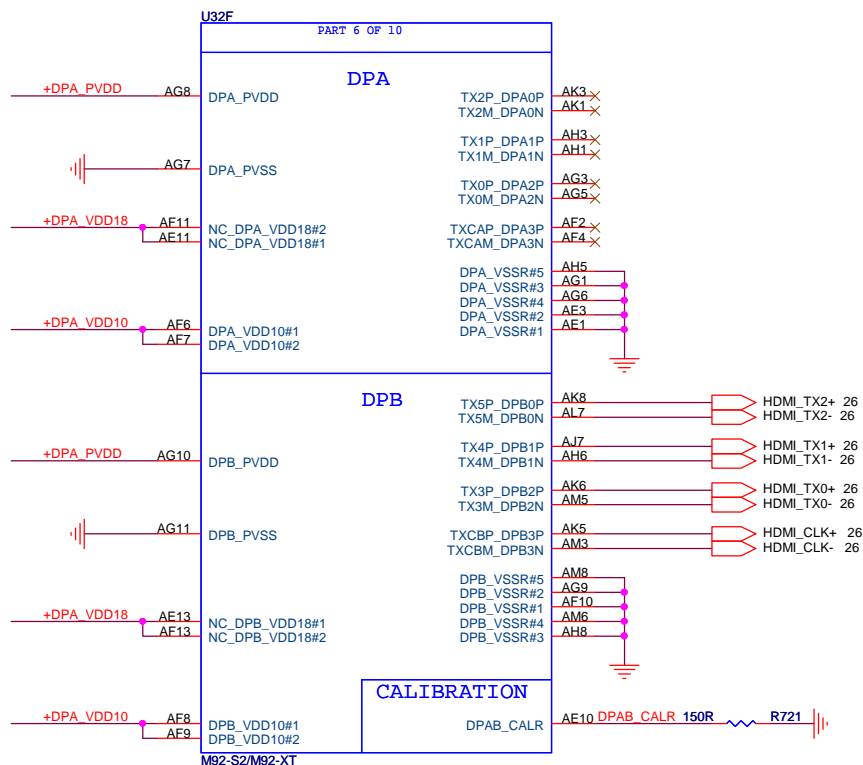
M92 thermal monitor change external to internal. 10/20







TMDP(HDMI) INTERFACE




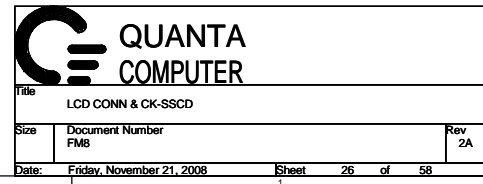
QUANTA COMPUTER

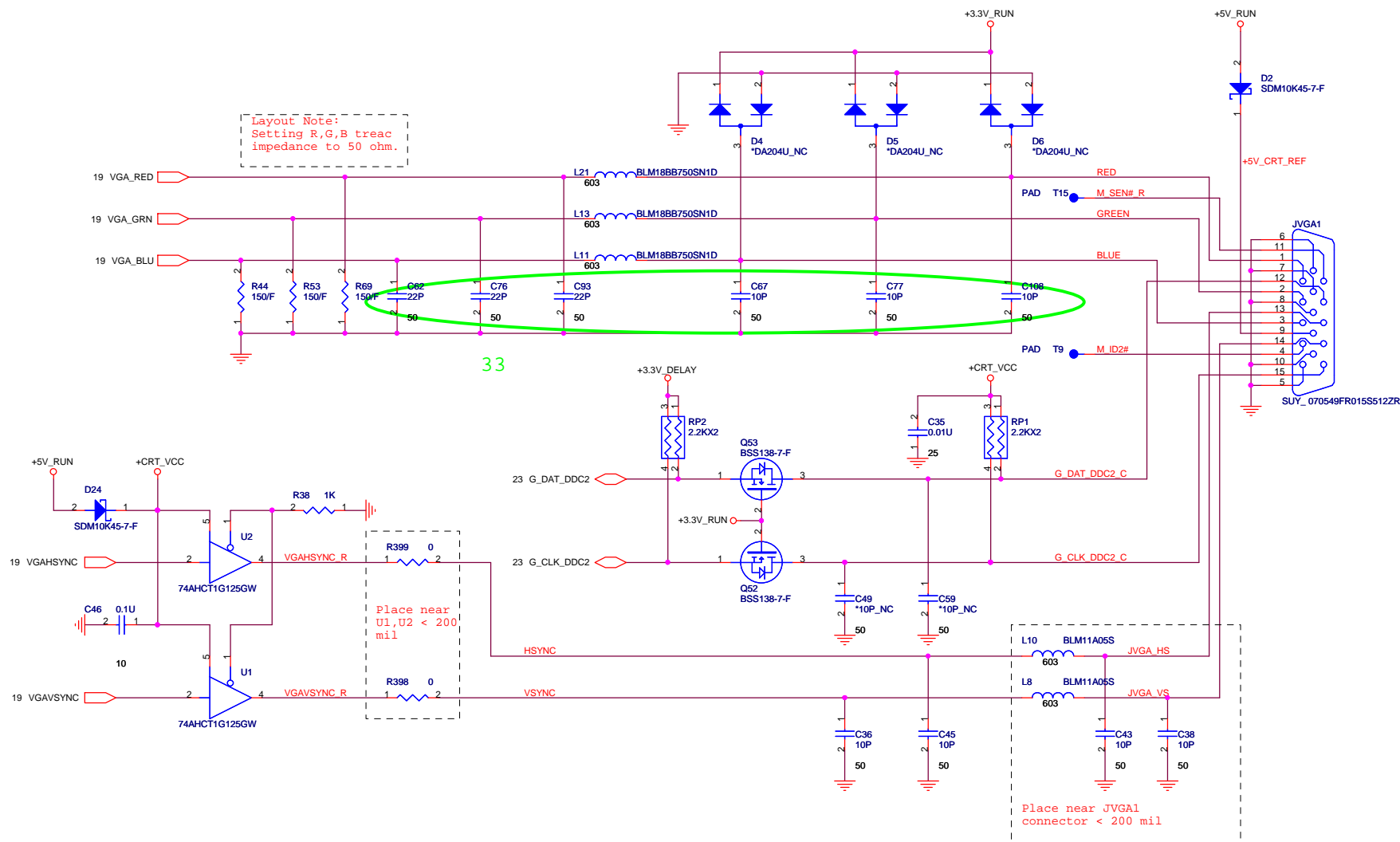
Title: VGA-M92-XT (PCIe)

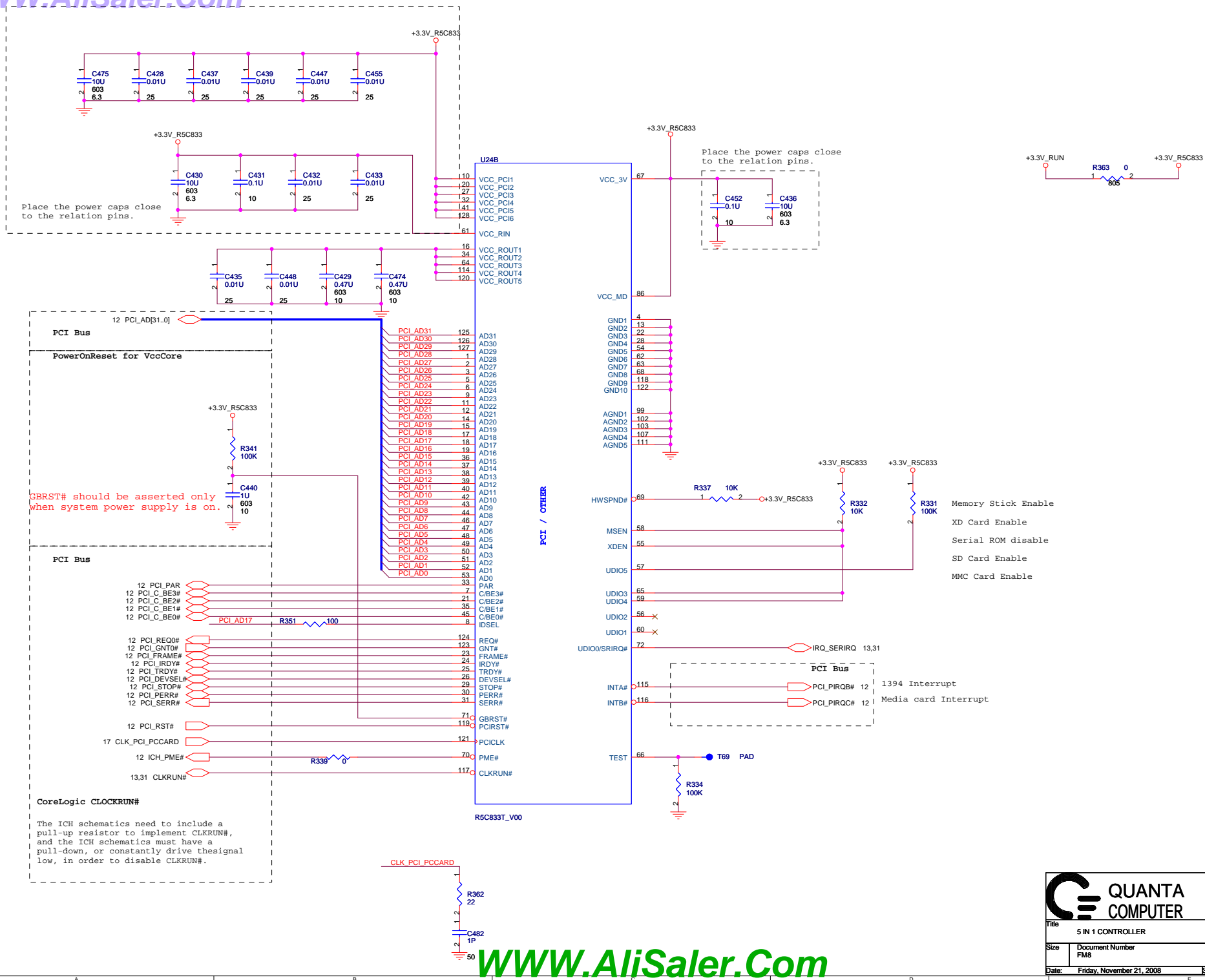
Size: Document Number FM8 Rev 2A

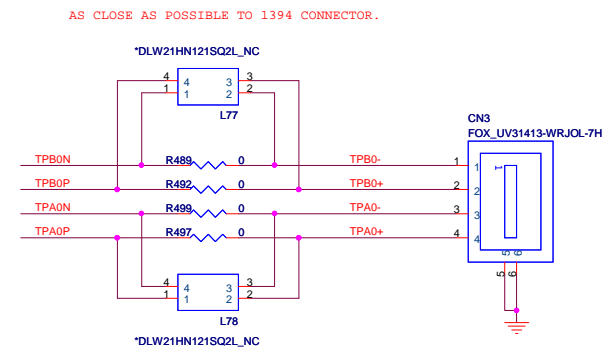
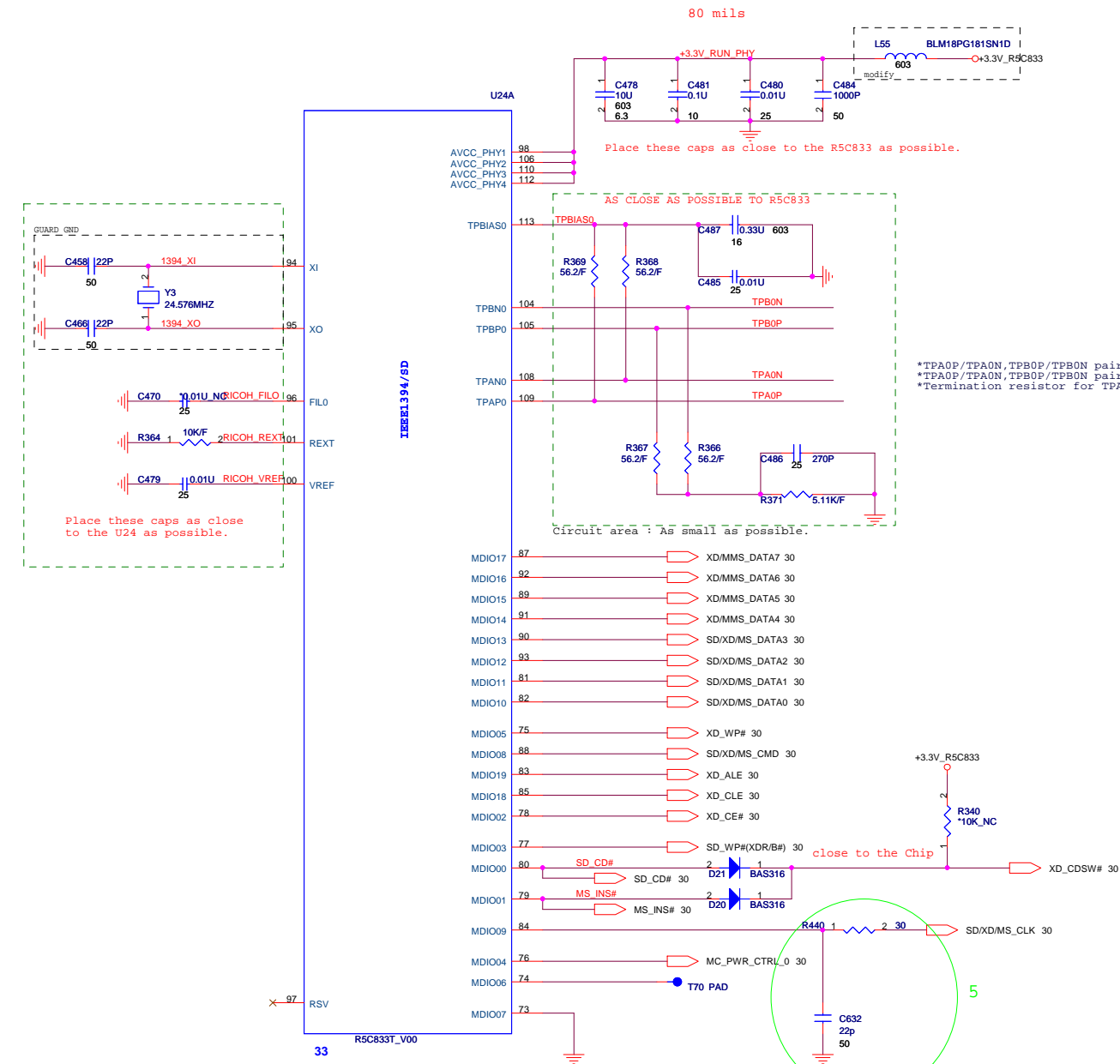
Date: Friday, November 21, 2008 Sheet 24 of 58

 QUANTA COMPUTER		
File: VGA-M82-S (PCIe)		
Size:	Document Number FM8	Rev 2A
Date:	Friday, November 21, 2008	Sheet 25 of 58



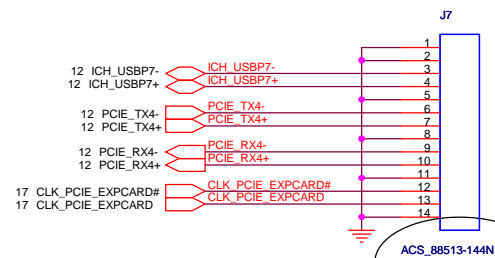
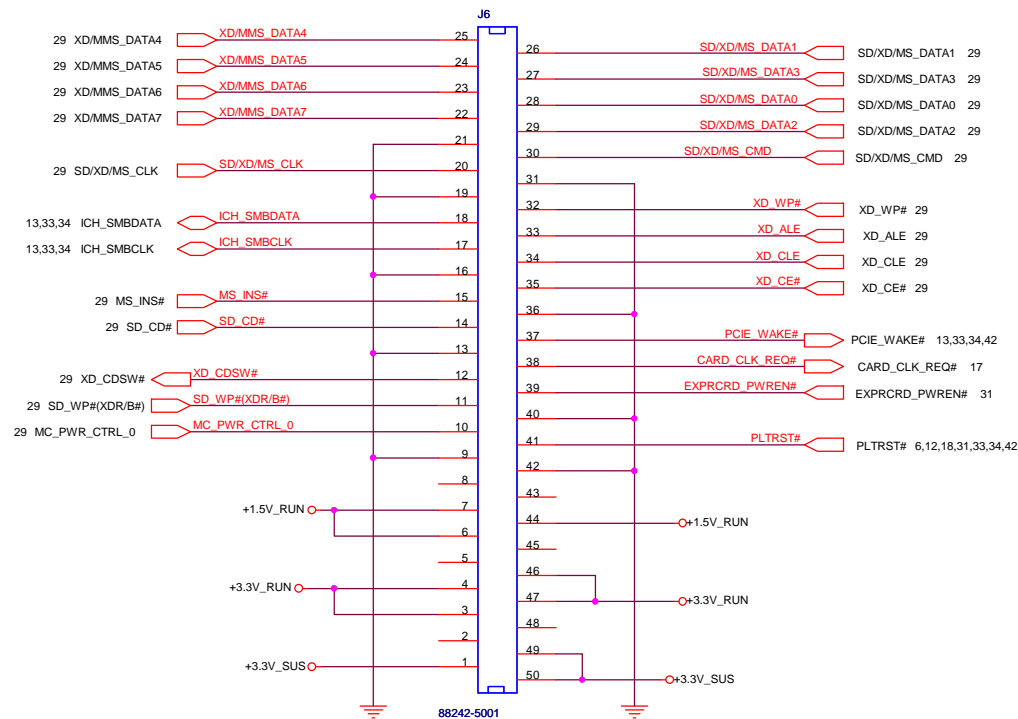






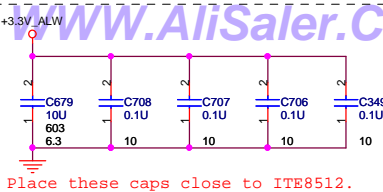
*TPA0P/TPA0N,TPB0P/TPB0N pair trace : As close as possible.
 *TPA0P/TPA0N,TPB0P/TPB0N pair trace : Same length electrically.
 *Termination resistor for TPA+/- TPB+/- : As close as possible to its cable driver (device pin out).

Express Card/CARD READER



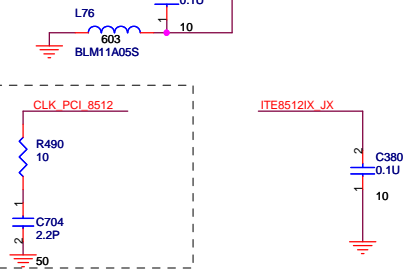
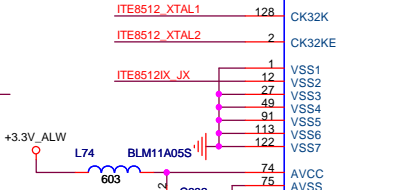
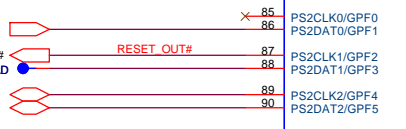
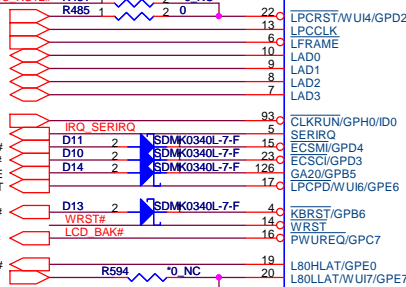
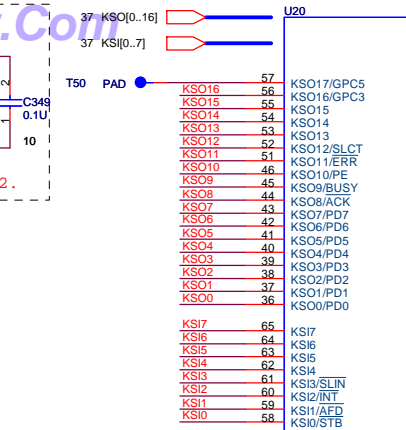
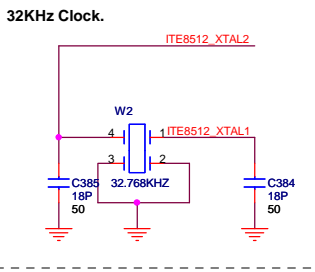
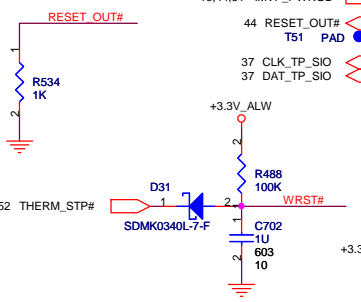
8/28:change PN to 88513-144N

Title: ExpressCard/SmartCard		
Size: FMS	Document Number: FMS	Rev: 2A
Date: Friday, November 21, 2008	Sheet: 30	of 58



Place these caps close to ITE8512.

Charge and BAT
CLK, LCD and Thermal
G_Thermal
and Media button



ITE8512E LQFP-128L

KEYBOARD

ADC/DAC

PWM

IR/UART

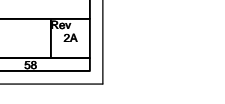
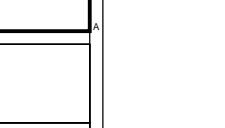
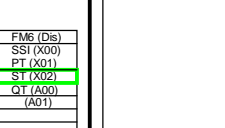
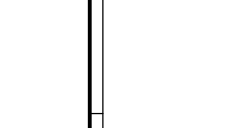
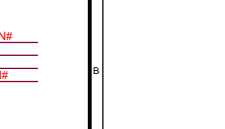
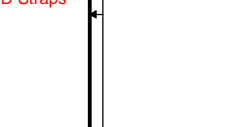
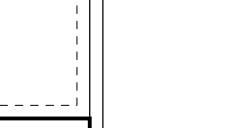
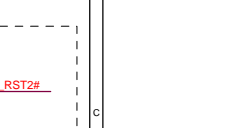
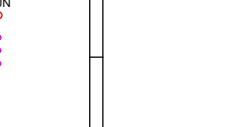
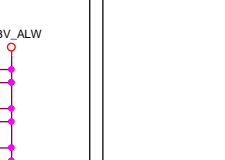
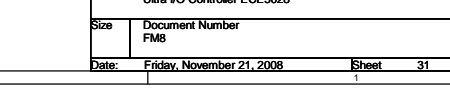
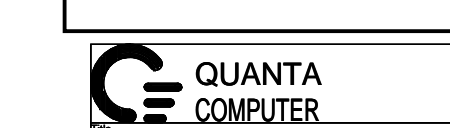
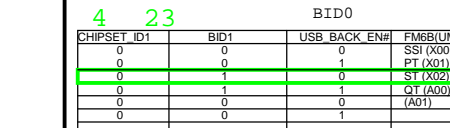
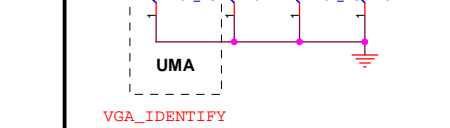
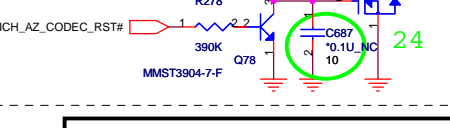
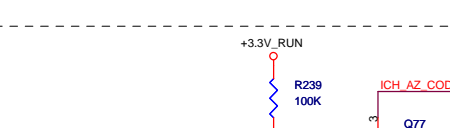
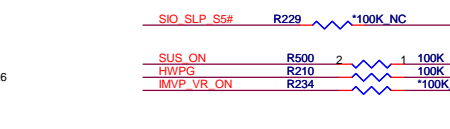
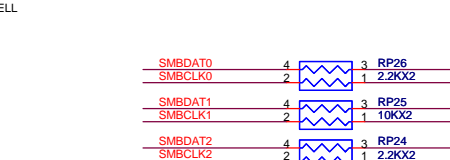
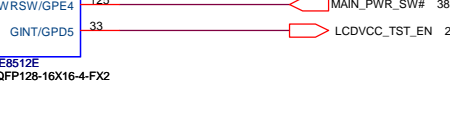
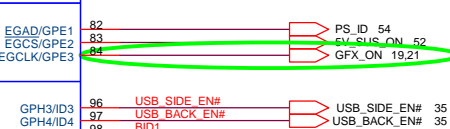
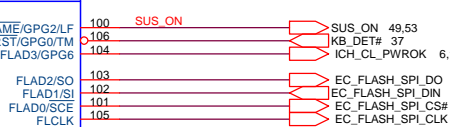
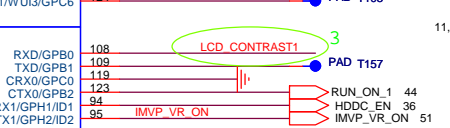
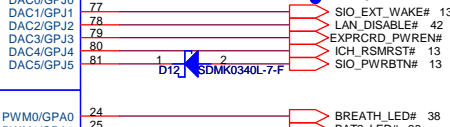
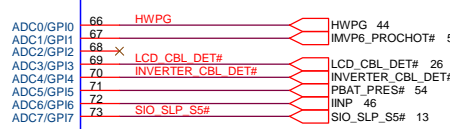
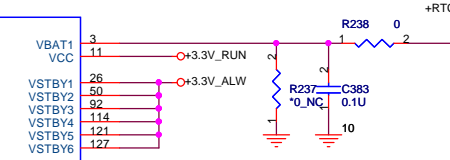
SMBUS

LPC/FW/FLASH

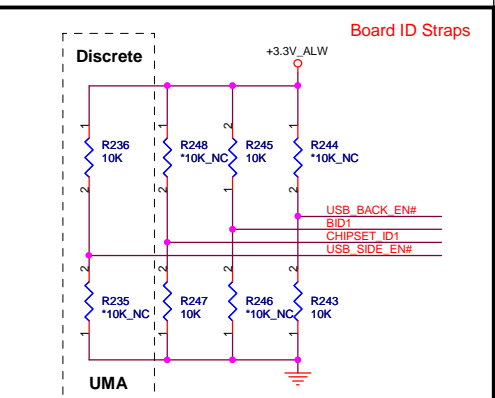
EGPC

GPIO

PS/2



(3)08/22: delete SM Bus and add contrast function



VGA_IDENTIFY

BID0

CHIPSET ID1	BID1	USB BACK_EN#	FM6B(UMA)	FM6(Ds)
0	0	0	SSI (X00)	SSI (X00)
0	0	1	PT (X01)	PT (X01)
0	1	0	ST (X02)	ST (X02)
0	1	1	QT (A00)	QT (A00)
0	0	0	(A01)	(A01)

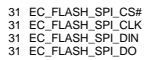
QUANTA COMPUTER

Ultra I/O Controller ECE5028

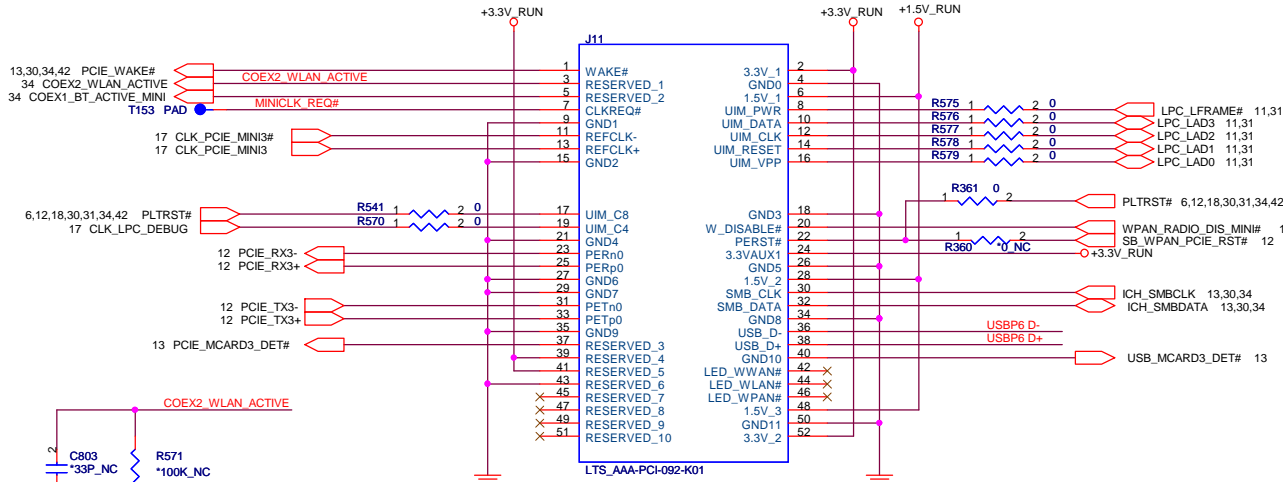
Size: Document Number: FMB

Date: Friday, November 21, 2008

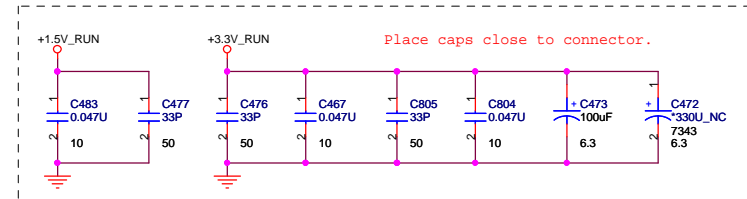
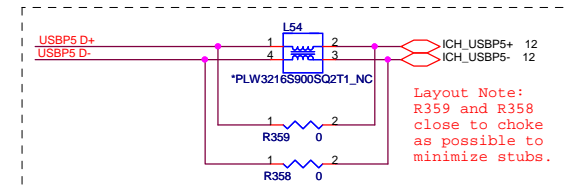
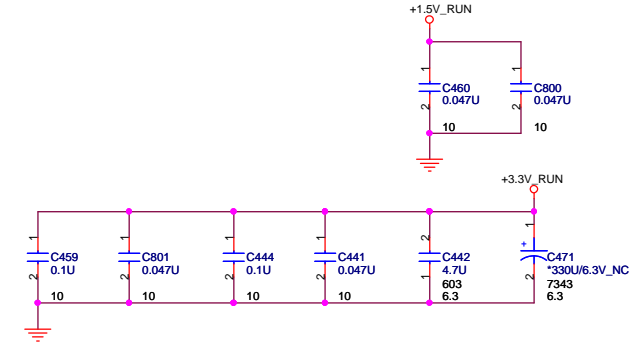
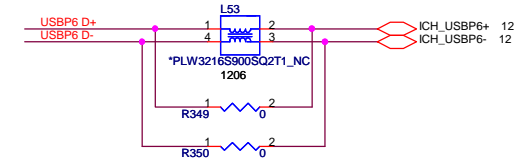
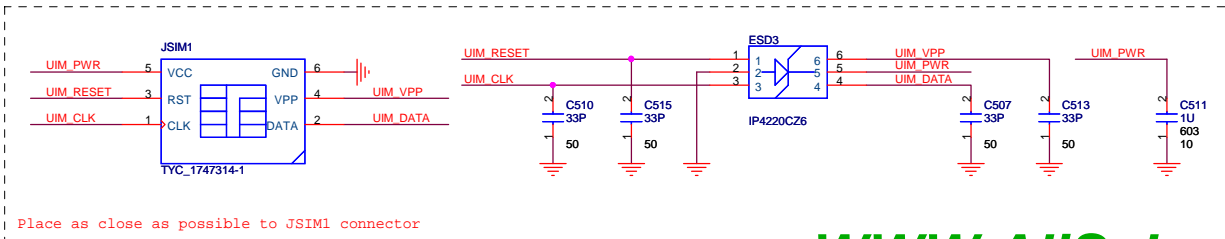
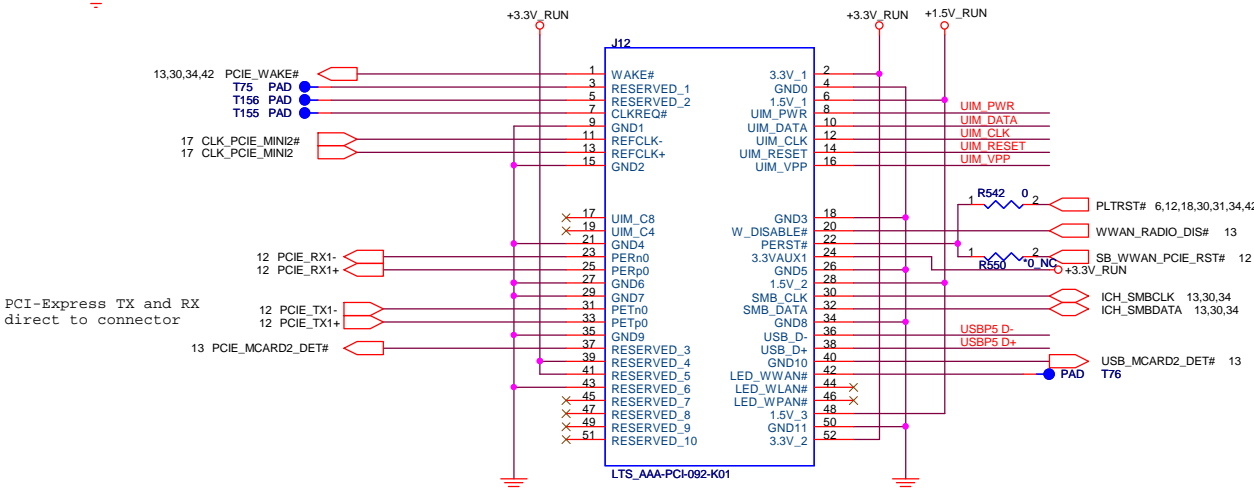
Sheet: 31 of 58



MiniCard Robson, BT. UWB connector

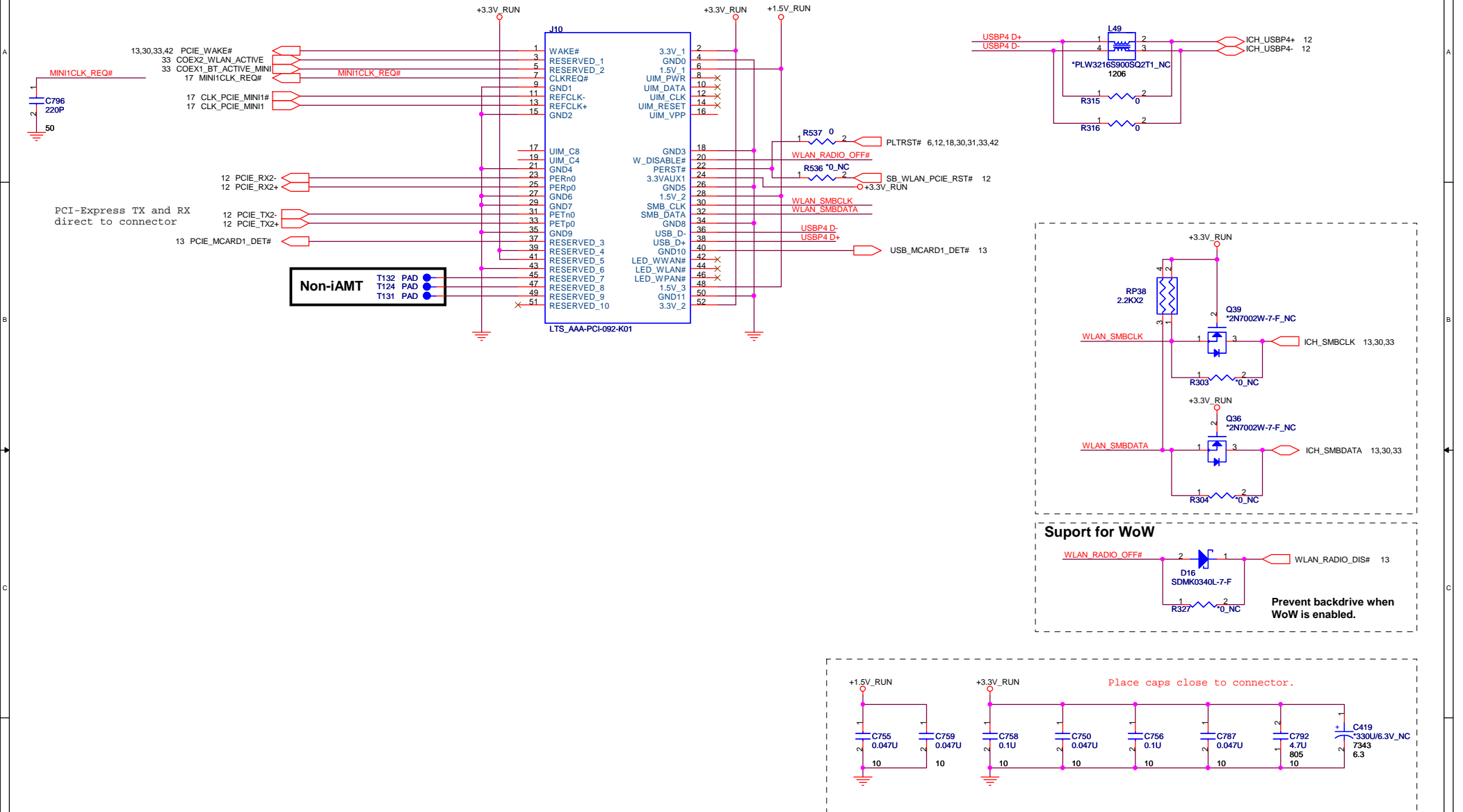


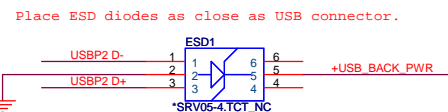
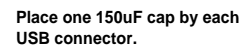
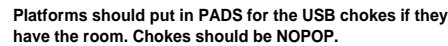
MiniCard WWAN connector



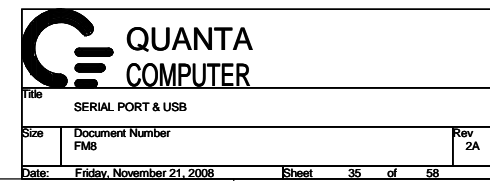
Title: MINI-PCI		
Size: FMS	Document Number: FMS	Rev: 2A
Date: Friday, November 21, 2008	Sheet: 33	of: 58

MiniCard WLAN connector

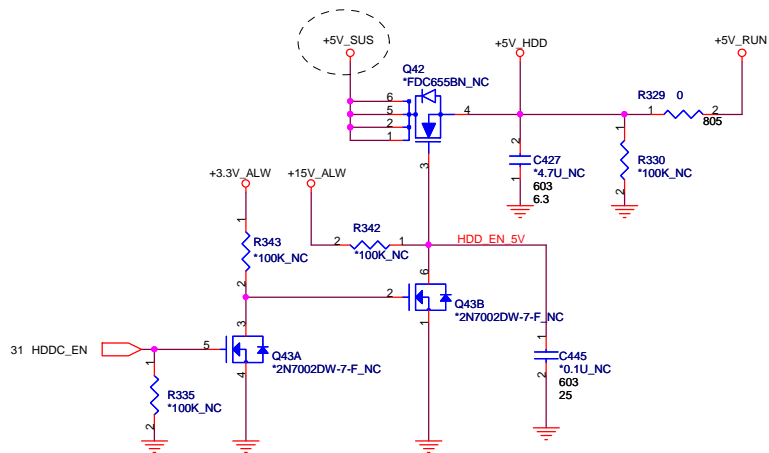
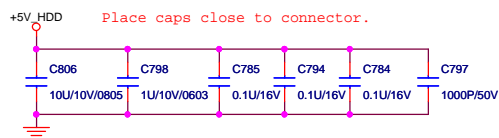
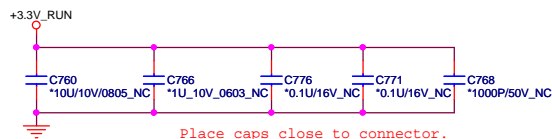
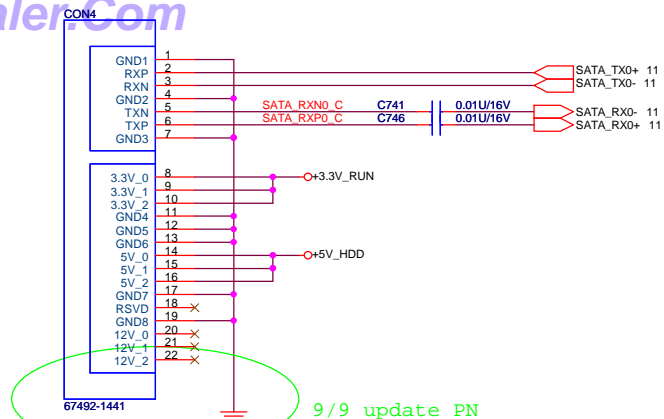




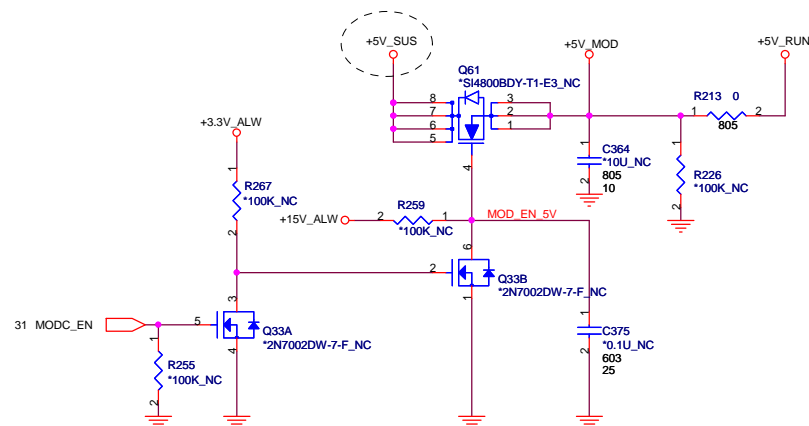
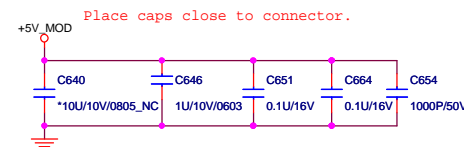
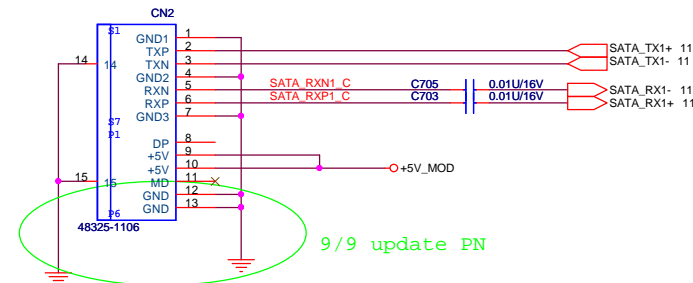
USBx2 & ESATA COMBO




SATA Connector.



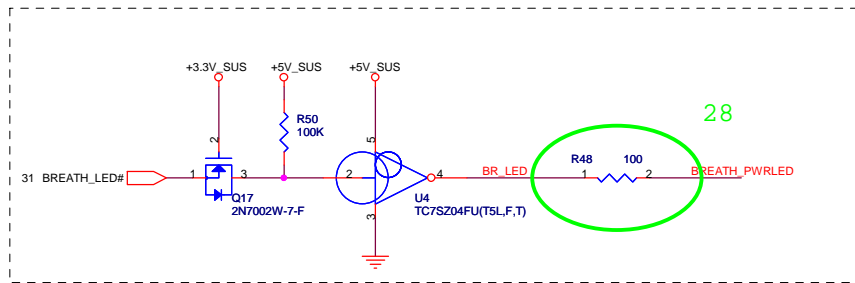
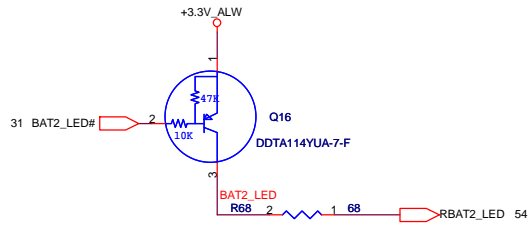
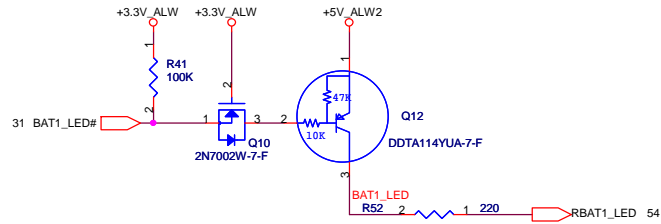
ODD Connector



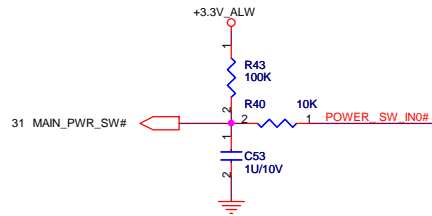
Title		
SATA (HDD&CD_ROM)		
Size	Document Number	Rev
FM8		2A
Date:	Friday, November 21, 2008	Sheet 36 of 58

 QUANTA COMPUTER			
Title TOUCH PAD, BULE TOOTH & FIR			
Size	Document Number FMS		Rev 2A
Date: Friday, November 21, 2008	Sheet	37	of 58

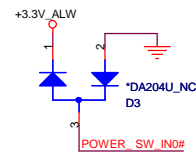
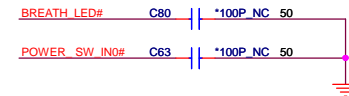
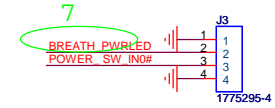
Battery status.

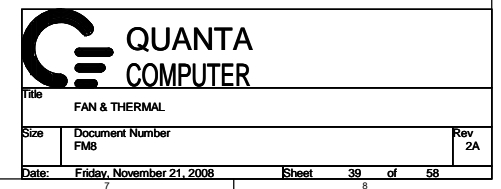



Power Switch

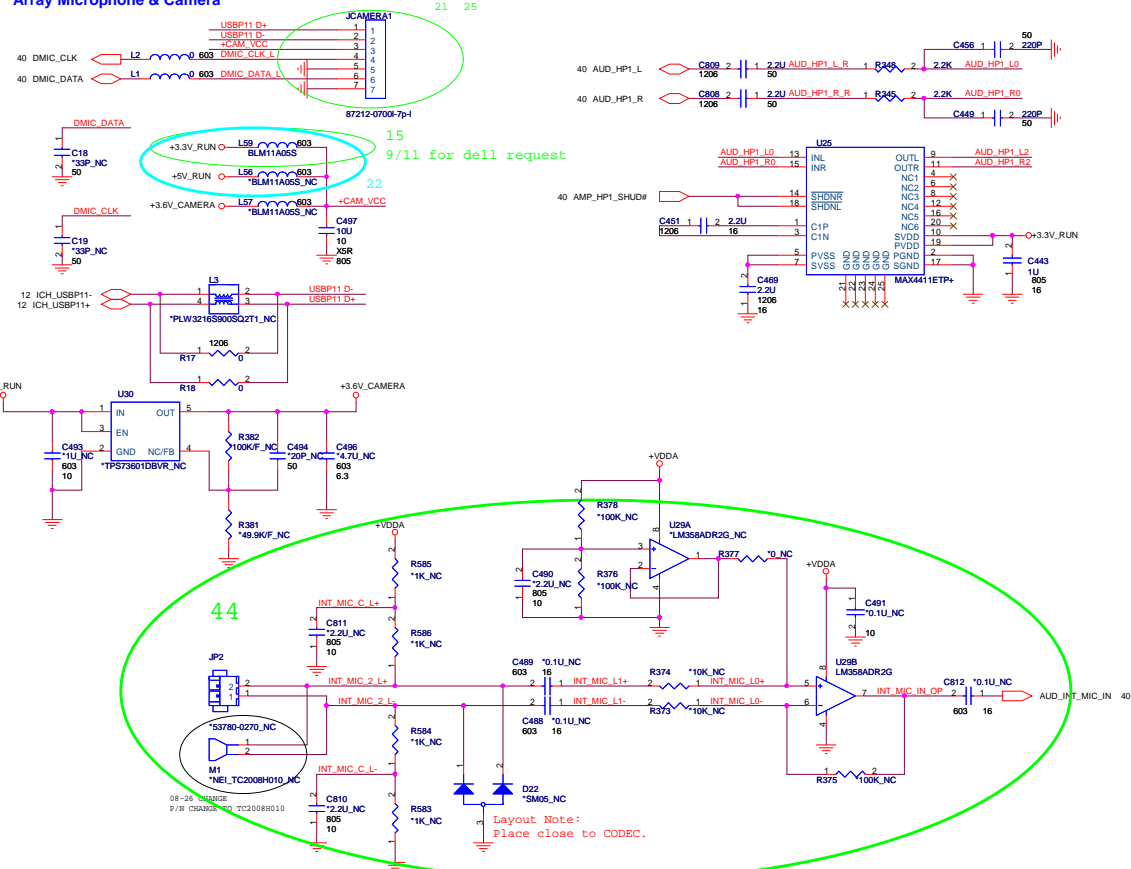
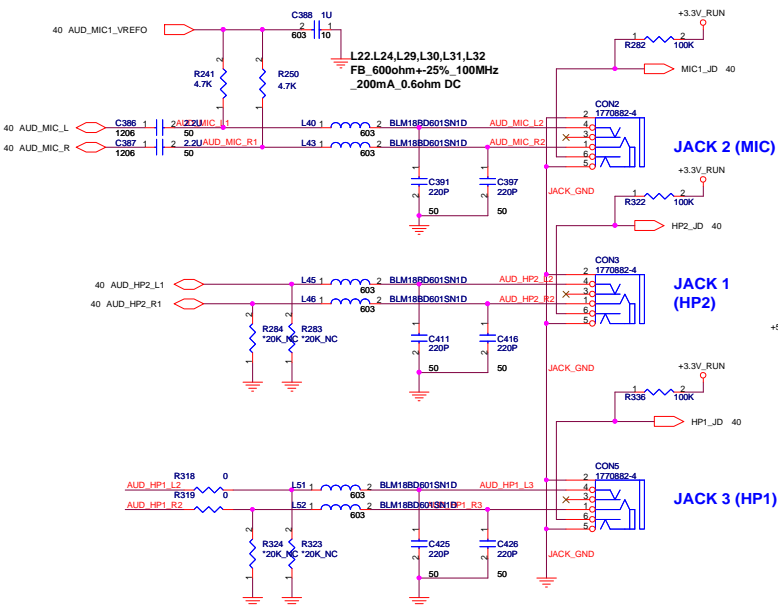


Power button cable



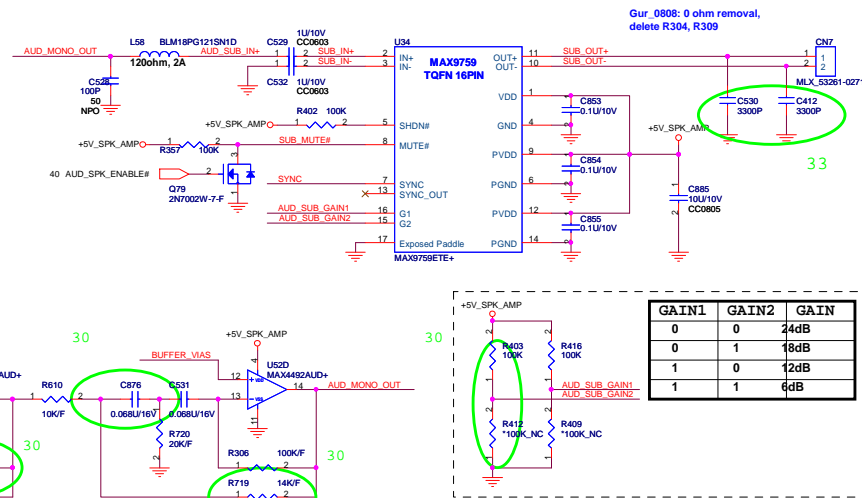


		QUANTA COMPUTER	
Title Azella CODEC			
Size	Document Number FmB		Rev 2A
Date: Friday, November 21, 2008		Sheet 40	of 58

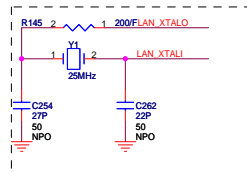
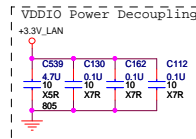
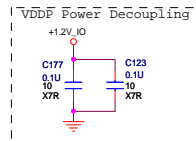
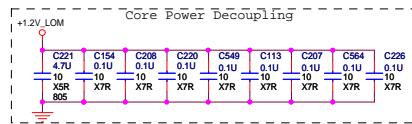


INTERNAL SUBWOOFER AMP

SYNC	Condition
VDD	Spread-spectrum mode with fS = 1200kHz \pm 70kHz.
GND	Fixed-frequency mode with fS = 1100kHz.
FLOAT	Fixed-frequency mode with fS = 1500kHz.
Clocked	Fixed-frequency mode with fS = external clock frequency.



GAIN1	GAIN2	GAIN
0	0	24dB
0	1	18dB
1	0	12dB
1	1	6dB



12 PCIE_RX6+GLAN_RX+
12 PCIE_RX6+GLAN_RX-
12 PCIE_TX6+GLAN_TX+
12 PCIE_TX6+GLAN_TX-
13,30,33,34 PCIE_WAKE#
6,12,18,30,31,33,34 PLTRST#
12 SB_L0M_PCIE_RST#
17 CLK_PCIE_LOM#
17 CLK_PCIE_LOM#

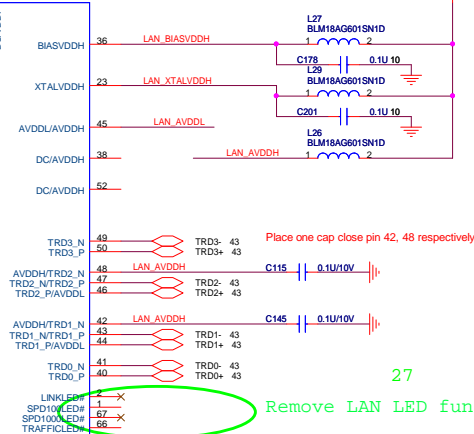
Gur_0331: change "LAN_DISABLE#" to "LAN_DISABLE" for high active

LAN_DISABLE is high active

Make sure it stays high when not driven by BCM5784M.

BCM5784M
10mm x 10mm
68-Pin QFN

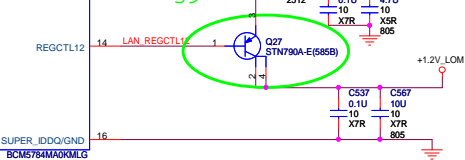
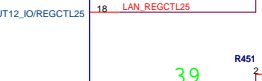
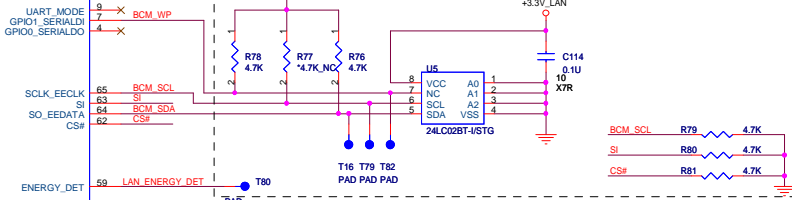
U9



27

Remove LAN LED function

R78 & R76: Stuff only if U5 is installed



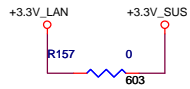
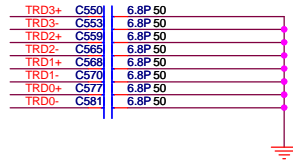
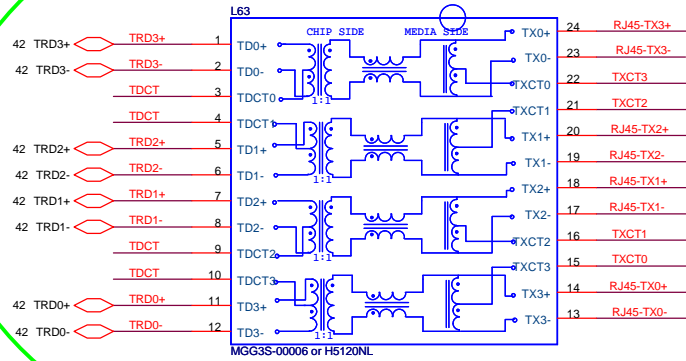
Note: thermal pad



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Rev	2A

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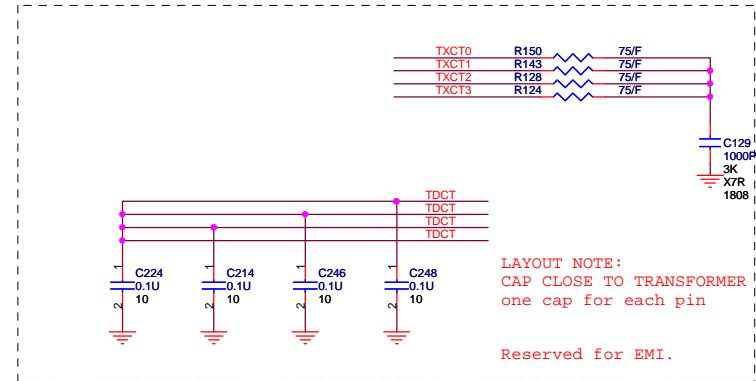
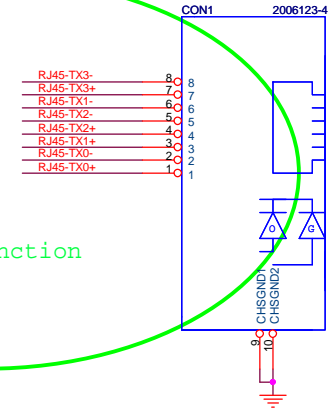
TRANSFORM



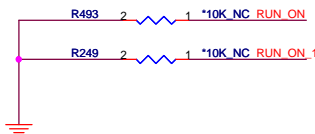
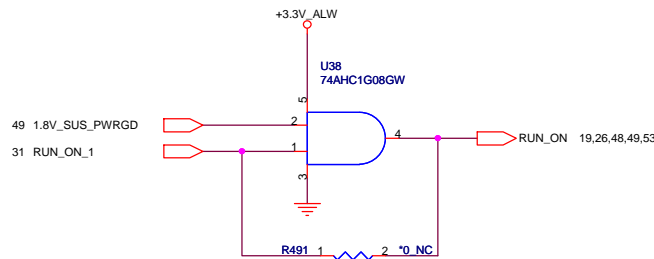
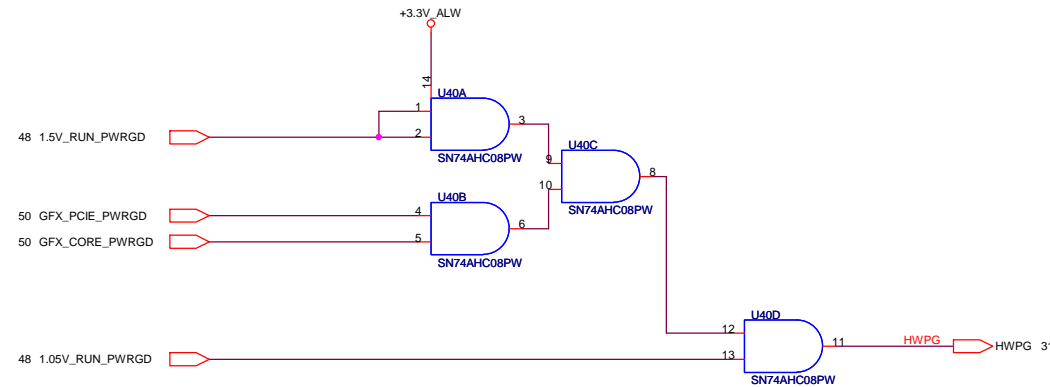
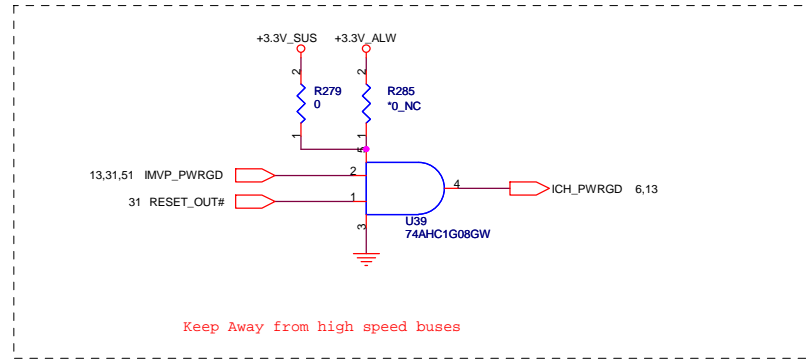
RJ-45 Connector


27


Remove LAN LED function

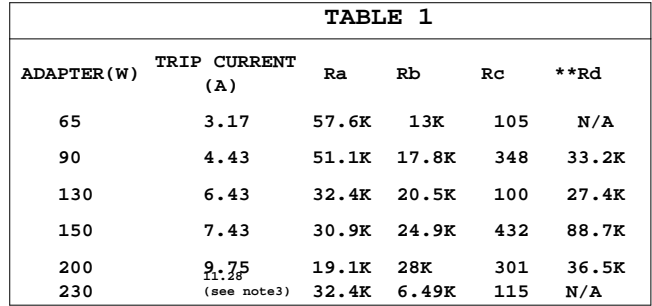


Title		
LAN SWITCH		
Size	Document Number	Rev
FM8		2A
Date:	Friday, November 21, 2008	Sheet 43 of 58




 QUANTA COMPUTER		
Title: System Reset Circuit		
Size: FMS	Document Number: FMS	Rev: 2A
Date: Friday, November 21, 2008	Sheet: 44	of 58

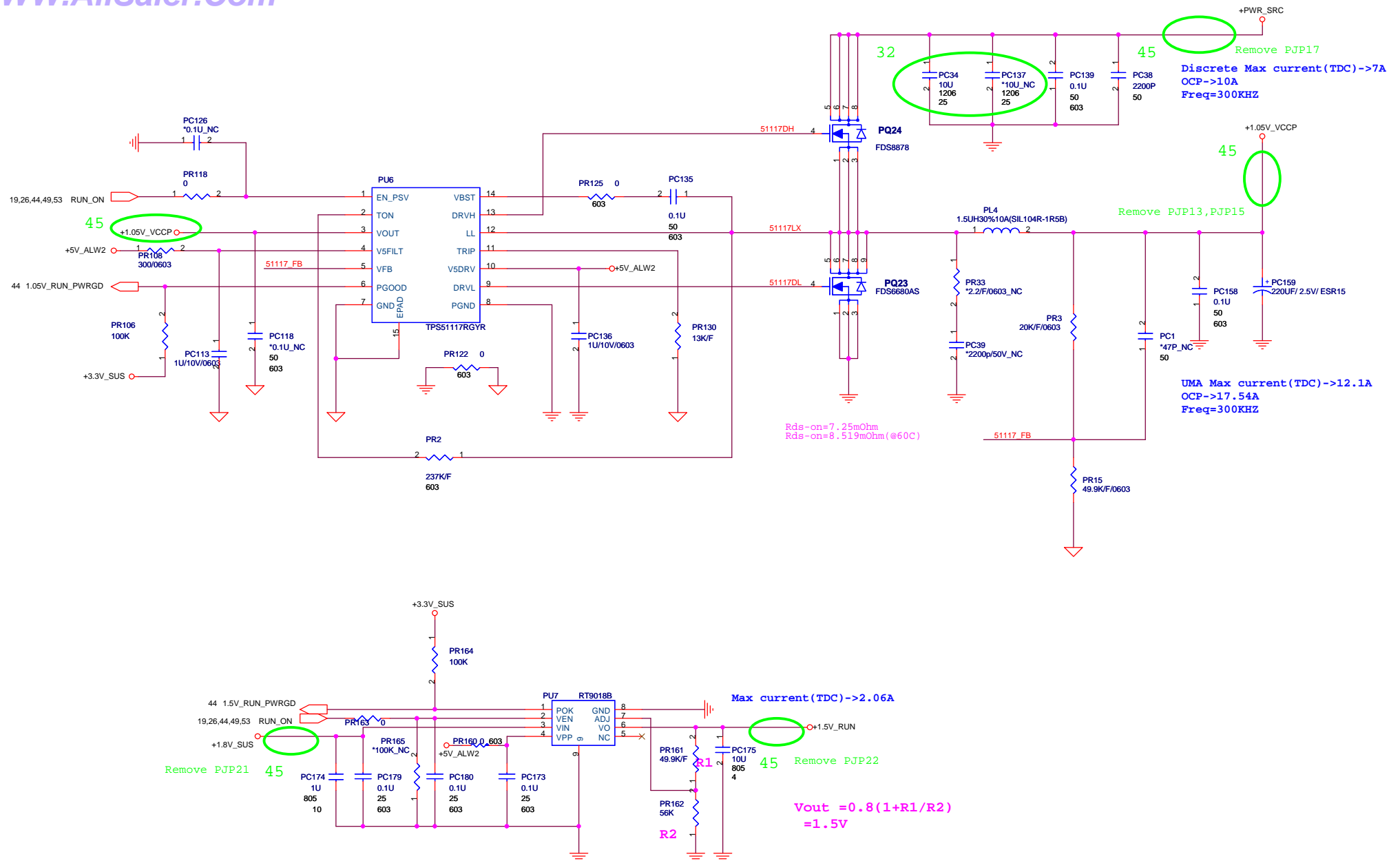
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Title Battery Selector		
Size	Document Number FM8	Rev 2A
Date:	Friday, November 21, 2008	Sheet 45 of 58

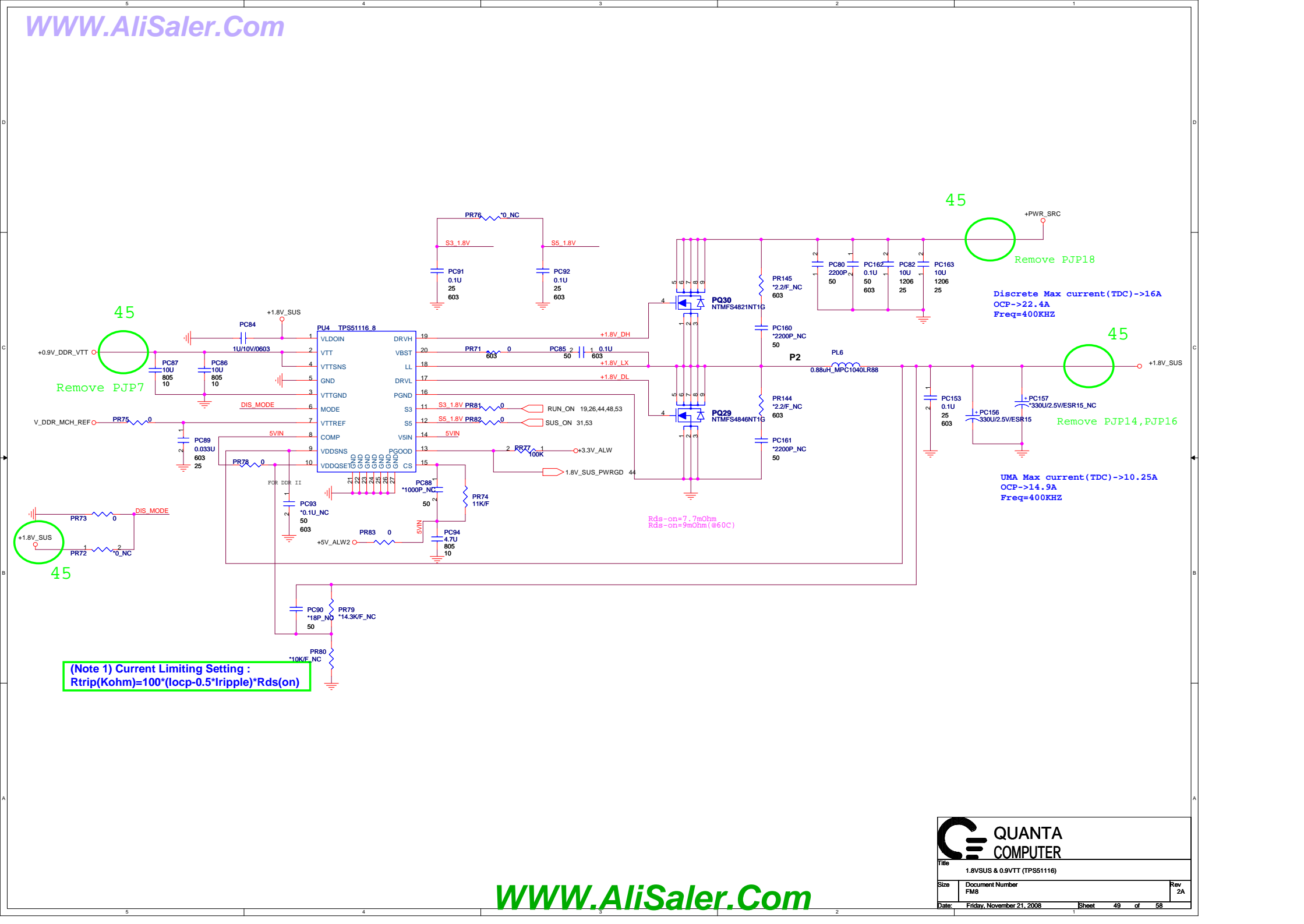


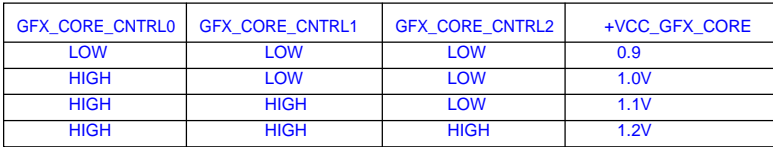
Note 3: PR35 must be 5mOhms instead of 10mOhms for the 230W adaptor.

**BLANK PAGE FOR PAGE
NUMBER SAME AS DISCRETE**

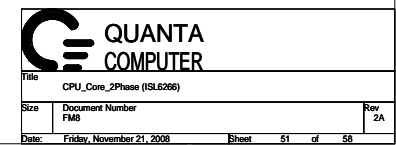
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Title			
Size	Document Number		Rev
	FM8		2A
Date:	Friday, November 21, 2008		Sheet 47 of 58

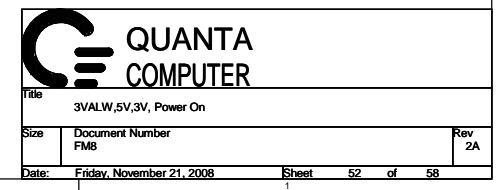


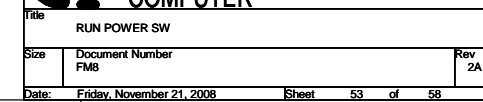
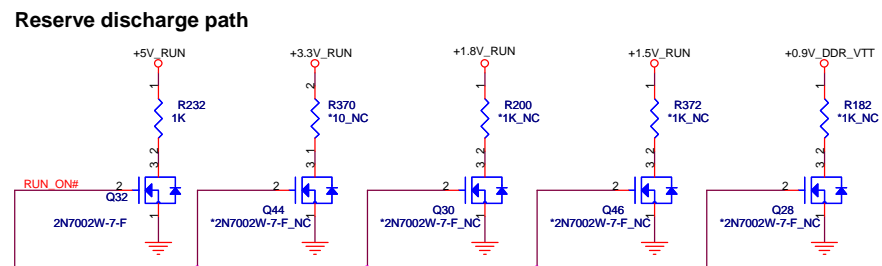
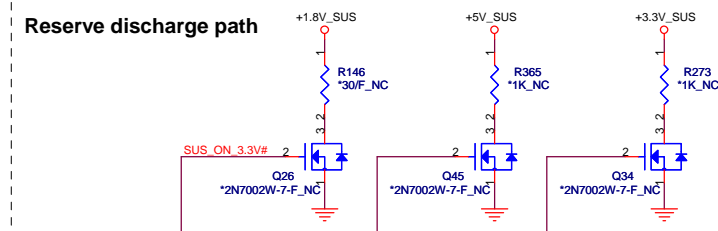
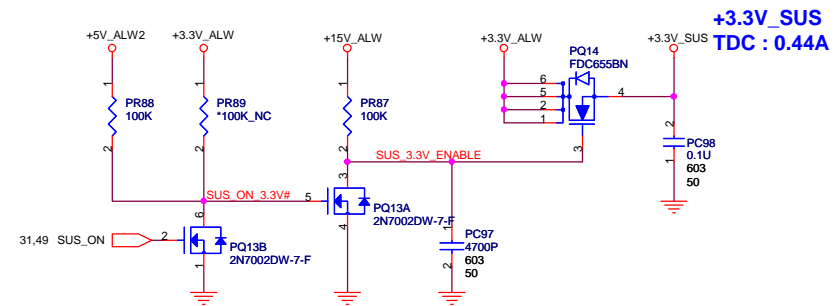


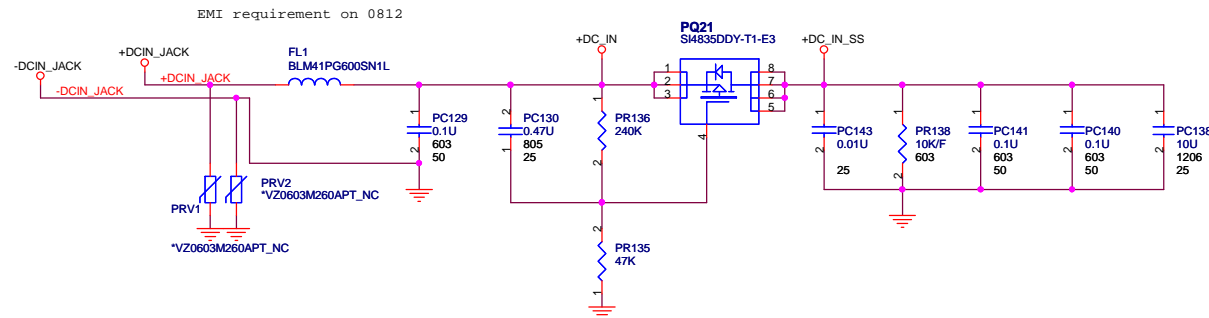
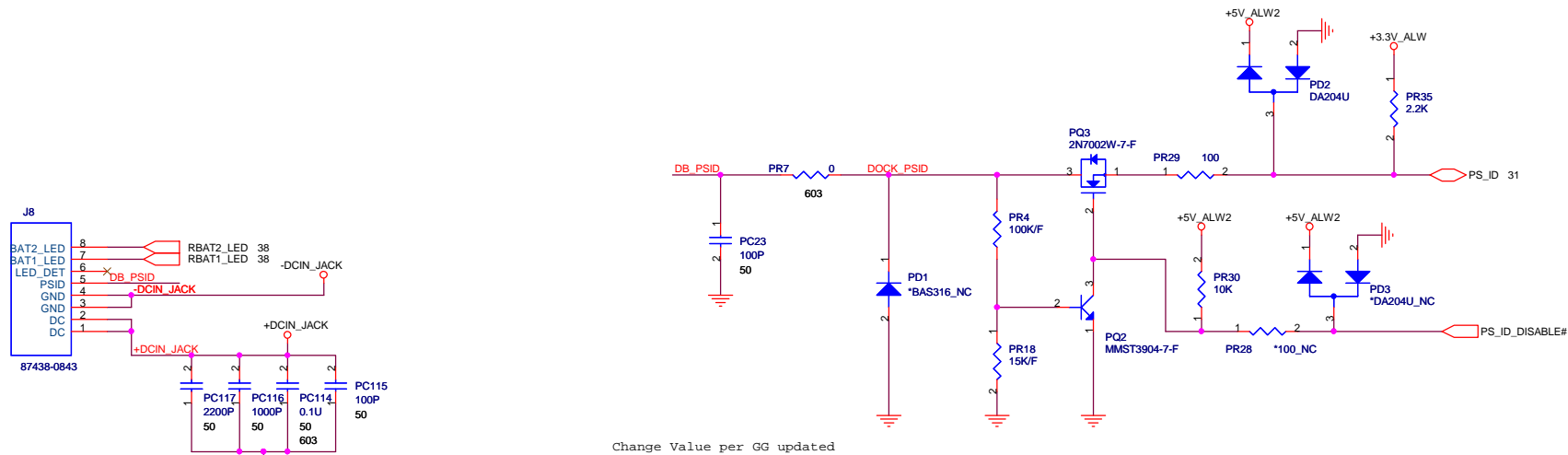
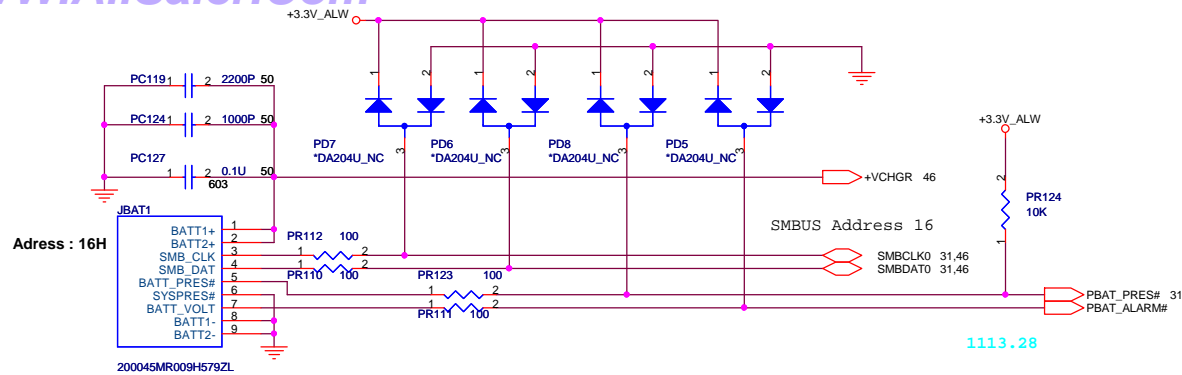


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VGA DC/DC			
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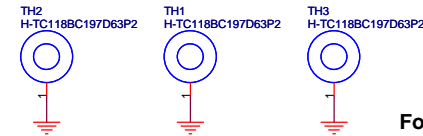
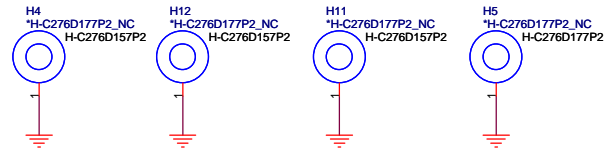




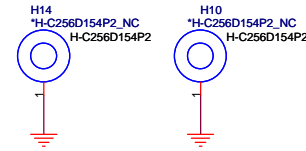
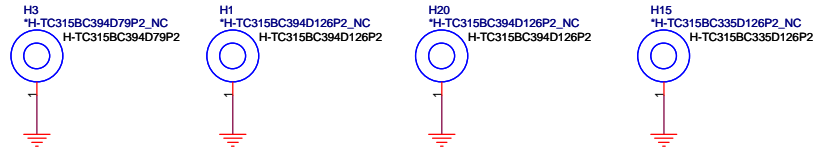




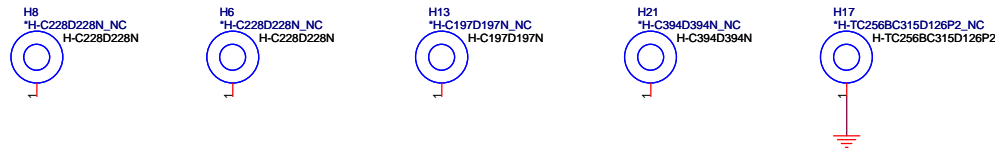
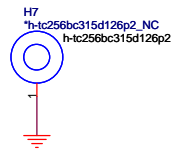
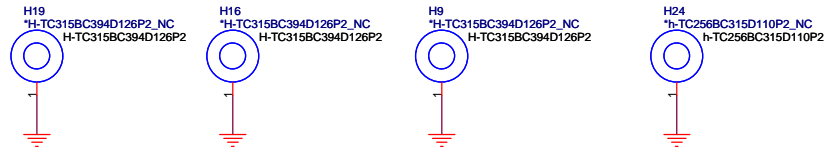
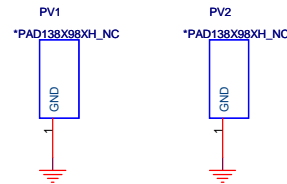
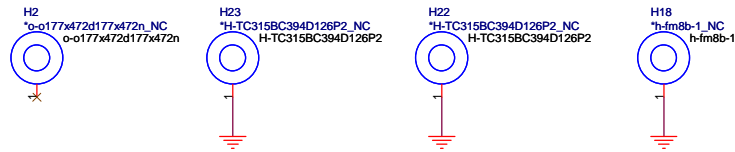
FOR CPU use




**For MiniCard nut use.
on 31' header**



For GPU nut use.



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 QUANTA COMPUTER		
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